This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Fig. 1

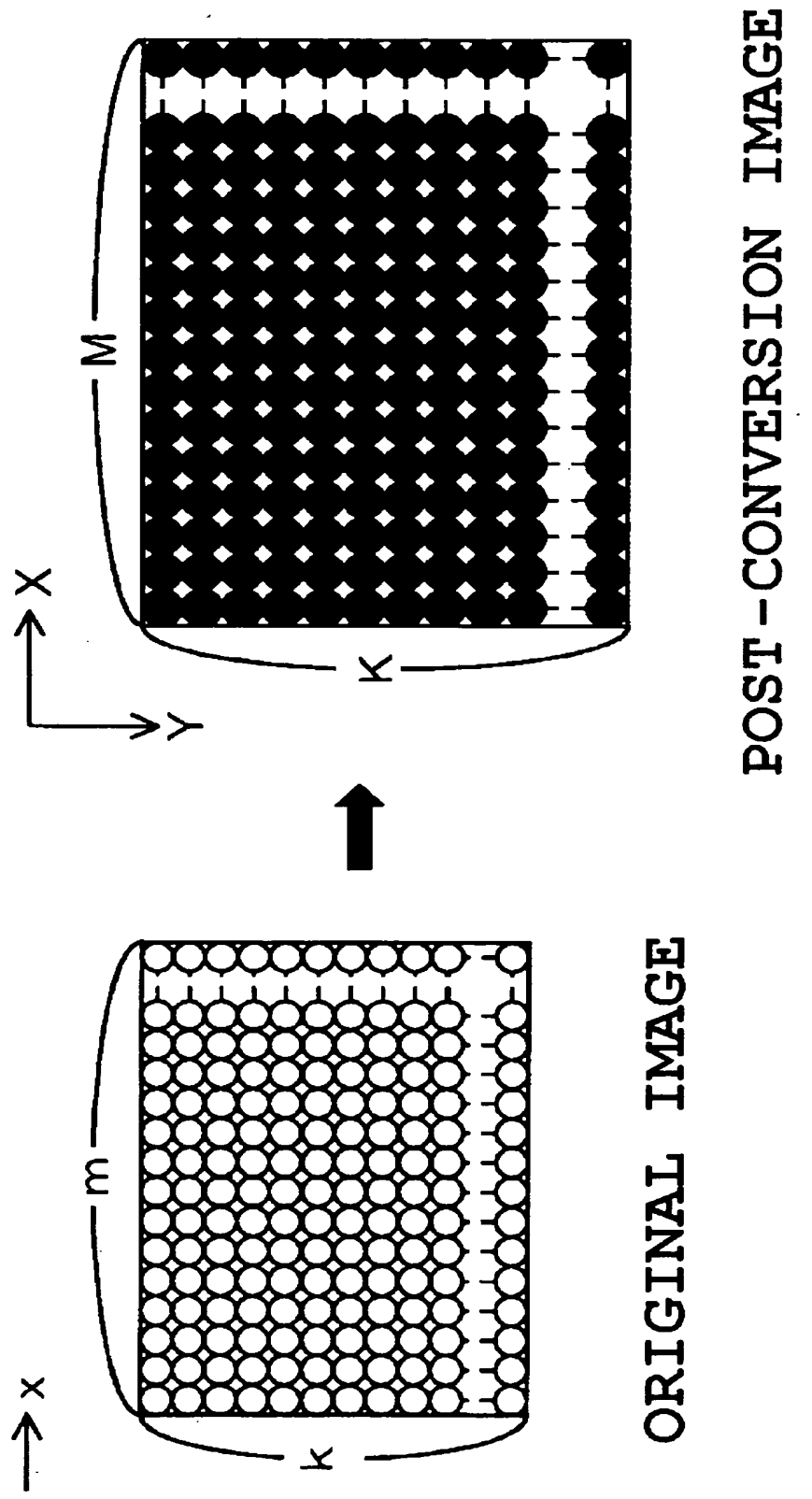


Fig. 2

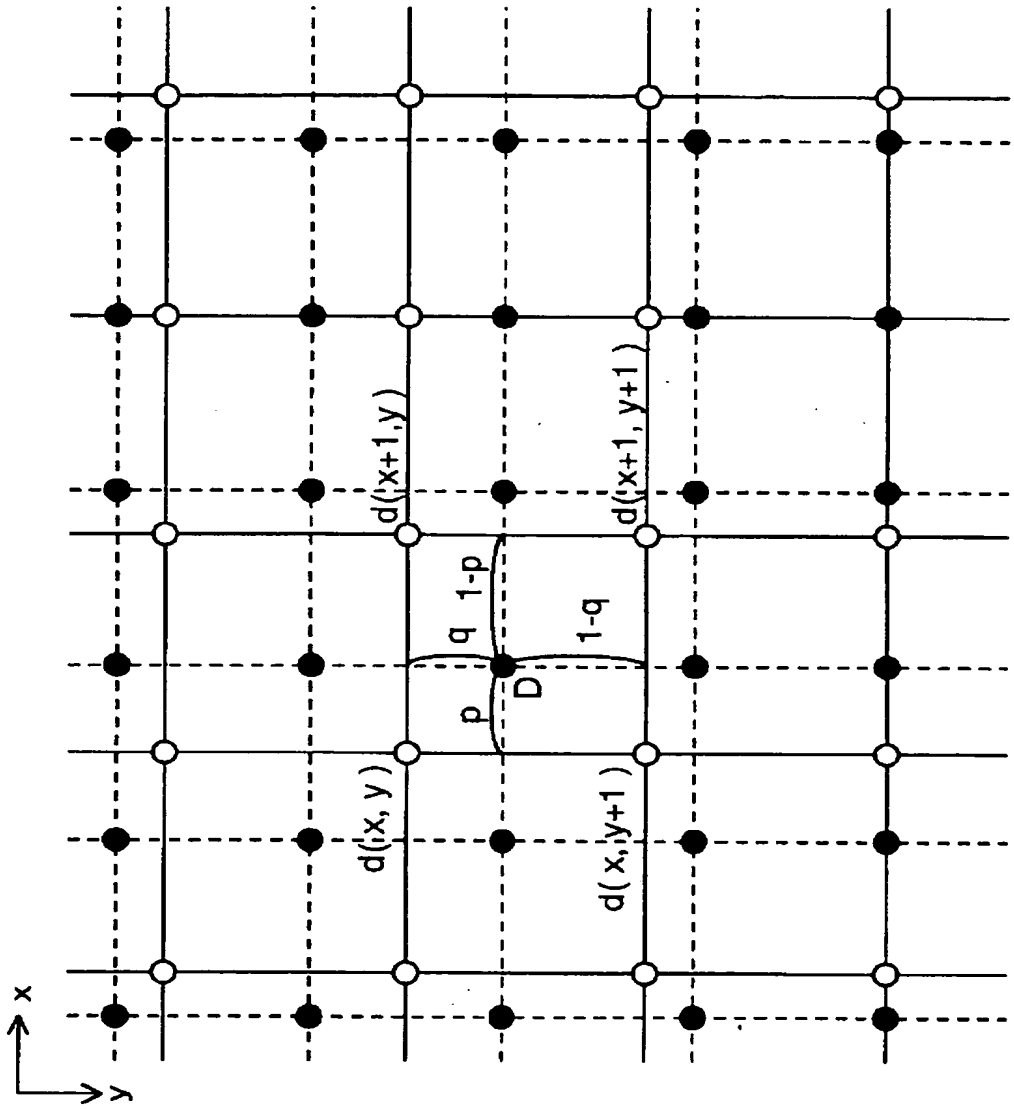


Fig. 3

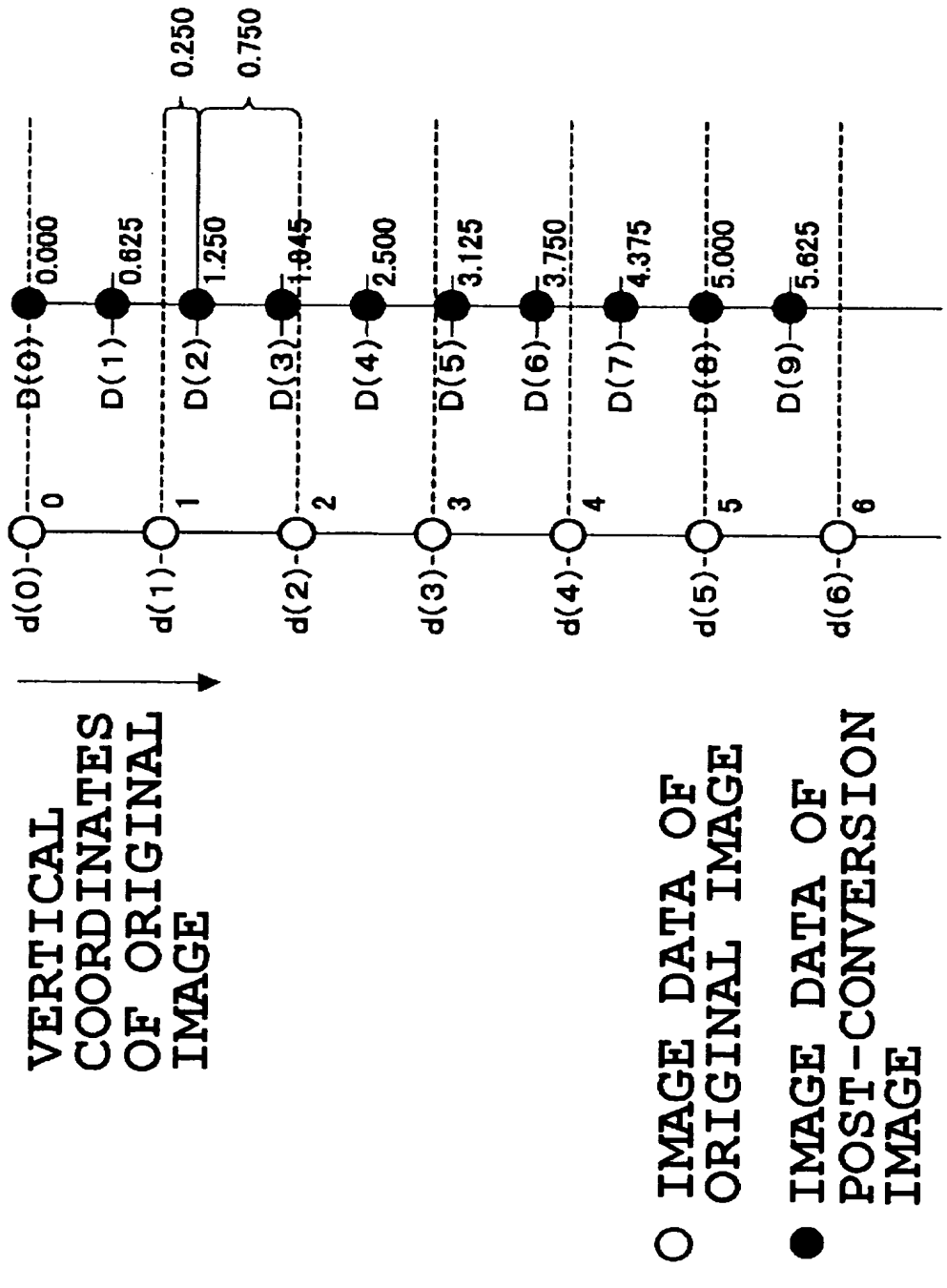

0.250
0.750
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)
D(8)
D(9)
0.000
0.625
1.250
1.875
2.500
3.125
3.750
4.375
5.000
5.625
d(0)
d(1)
d(2)
d(3)
d(4)
d(5)
d(6)
0
1
2
3
4
5
6
VERTICAL COORDINATES OF ORIGINAL IMAGE
○ IMAGE DATA OF ORIGINAL IMAGE
● IMAGE DATA OF POST-CONVERSION IMAGE

Fig. 4

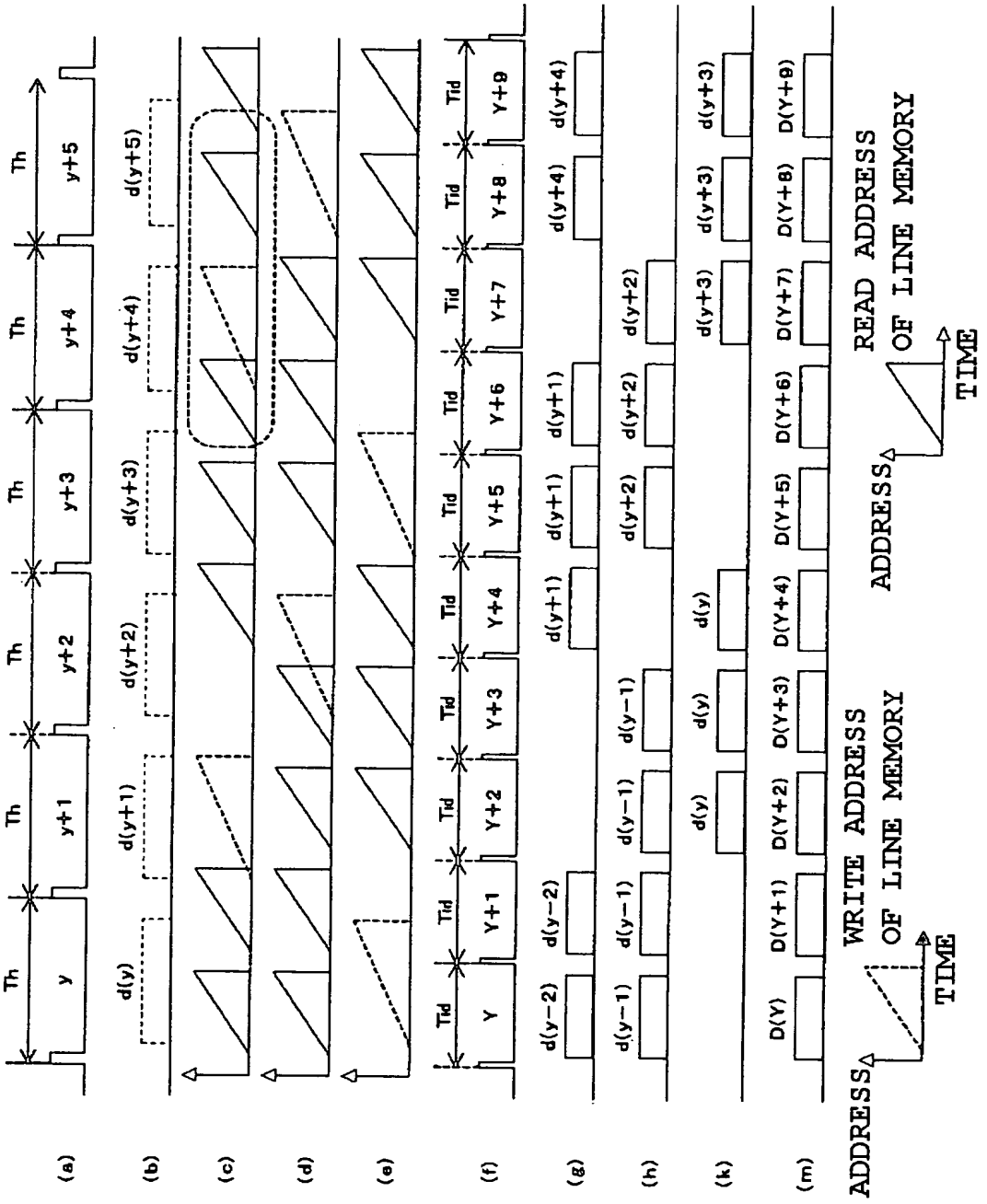

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(k)
(m)
Th
Tid
y
y+1
y+2
y+3
y+4
y+5
Y
Y+1
Y+2
Y+3
Y+4
Y+5
Y+6
Y+7
Y+8
Y+9
d(y)
d(y+1)
d(y+2)
d(y+3)
d(y+4)
d(y+5)
d(y-2)
d(y-1)
D(Y)
D(Y+1)
D(Y+2)
D(Y+3)
D(Y+4)
D(Y+5)
D(Y+6)
D(Y+7)
D(Y+8)
D(Y+9)
ADDRESS
WRITE ADDRESS
OF LINE MEMORY
TIME
ADDRESS
READ ADDRESS
OF LINE MEMORY
TIME

Fig. 5

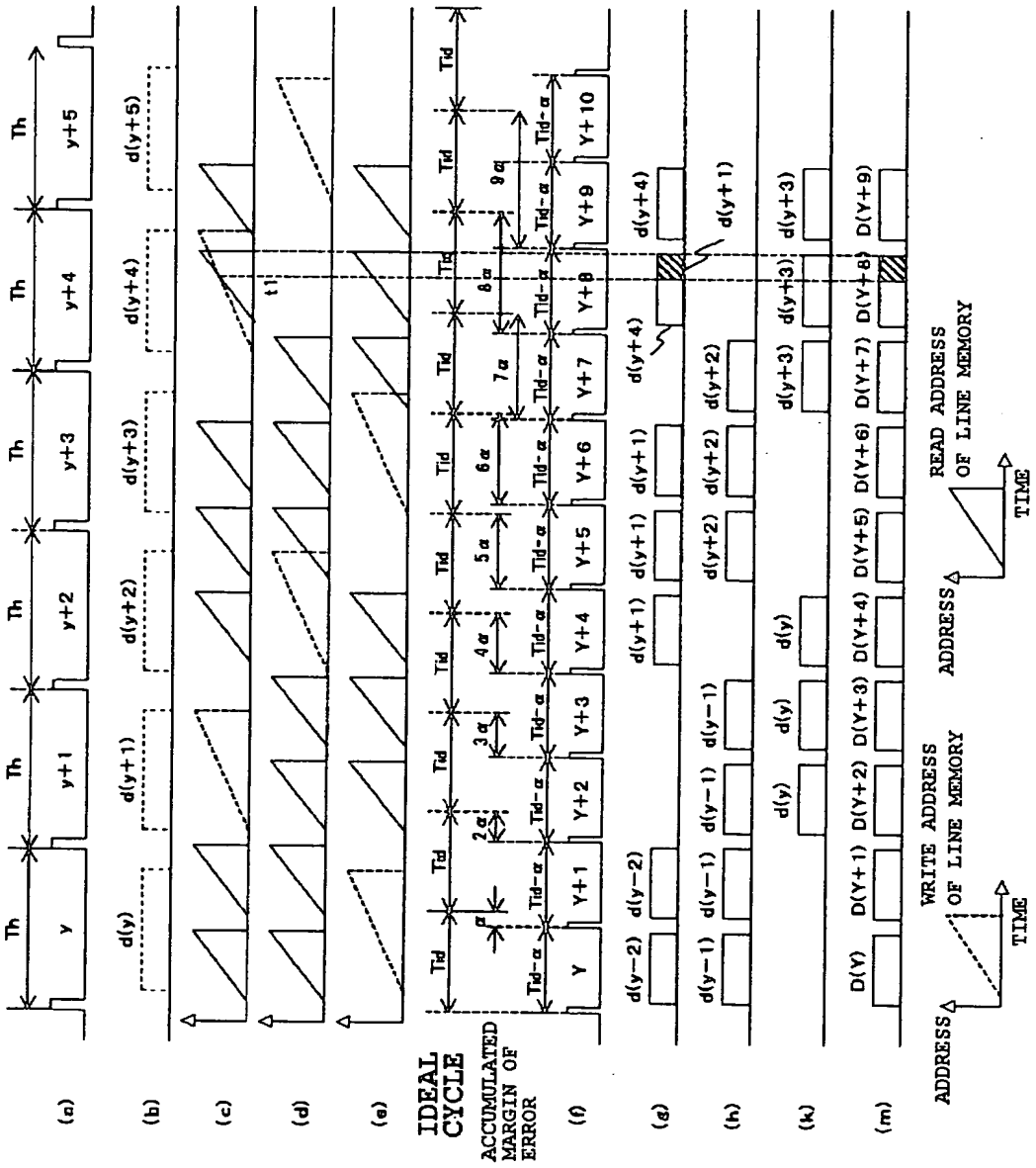

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(k)
(m)
IDEAL CYCLE
ACCUMULATED MARGIN OF ERROR
WRITE ADDRESS OF LINE MEMORY
READ ADDRESS OF LINE MEMORY
ADDRESS
TIME

Fig. 6

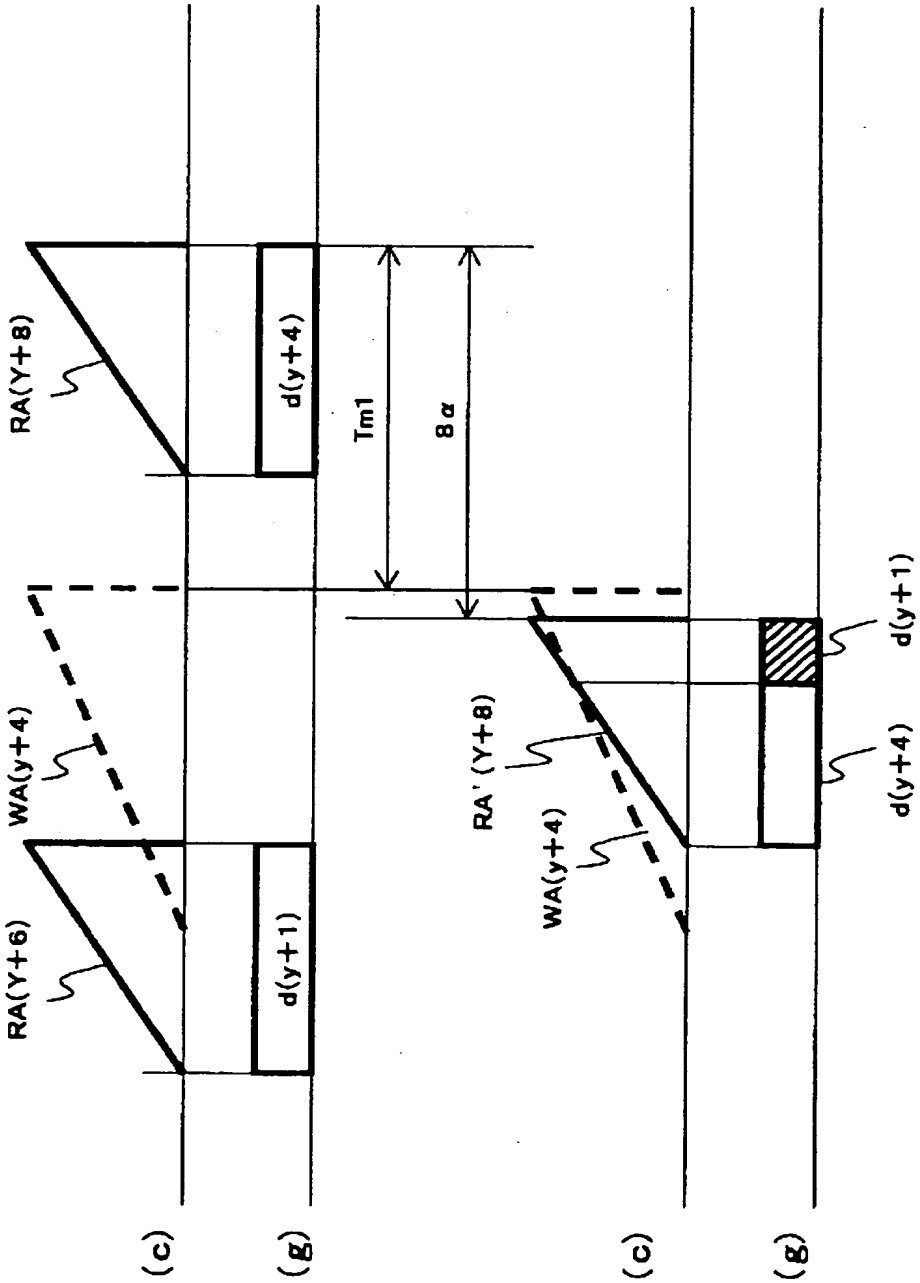


Fig. 7

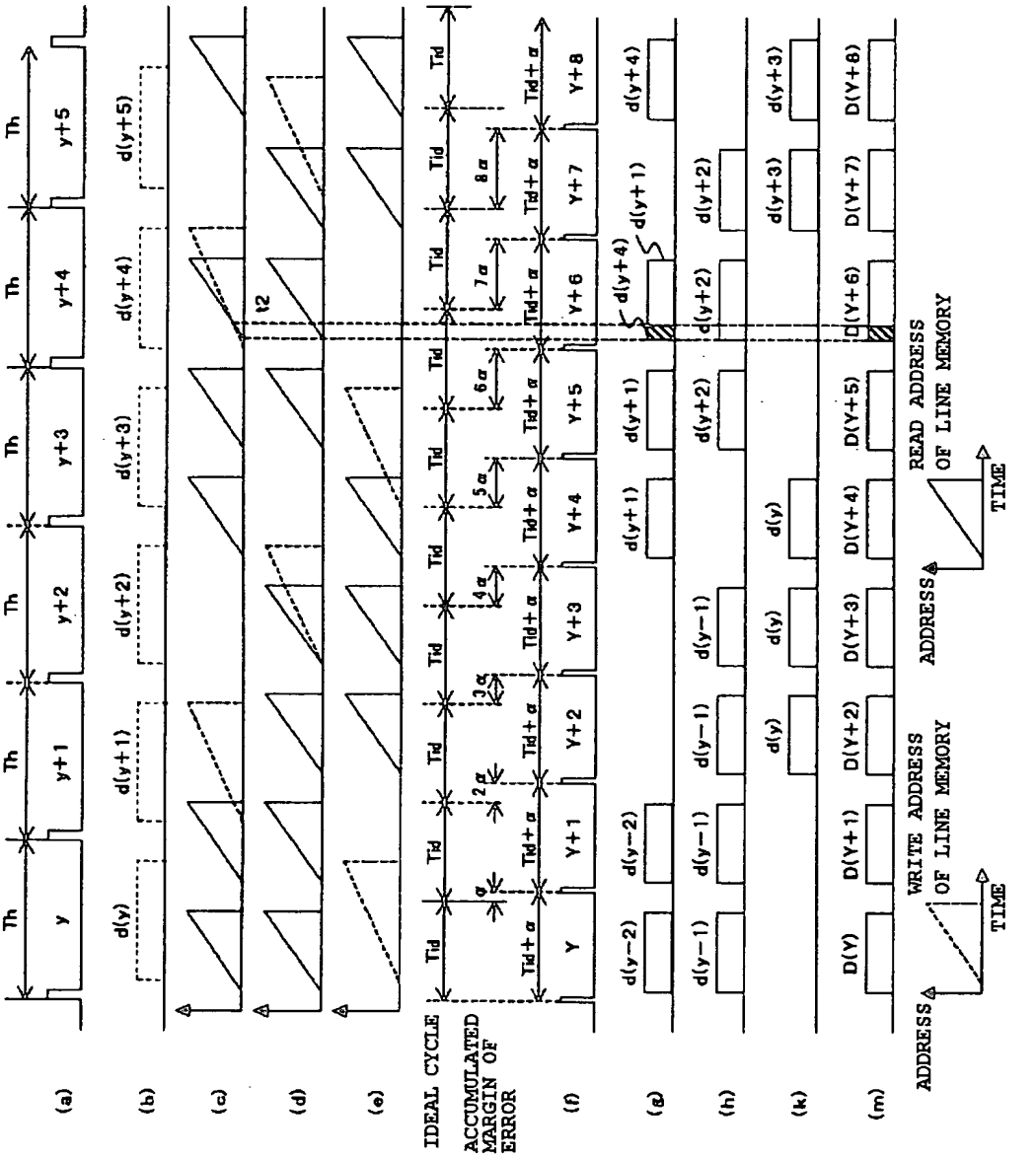

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(k)
(m)
IDEAL CYCLE
ACCUMULATED MARGIN OF ERROR
Th
Tid
Tid+α
WRITE ADDRESS OF LINE MEMORY
READ ADDRESS OF LINE MEMORY
ADDRESS
TIME

Fig. 8

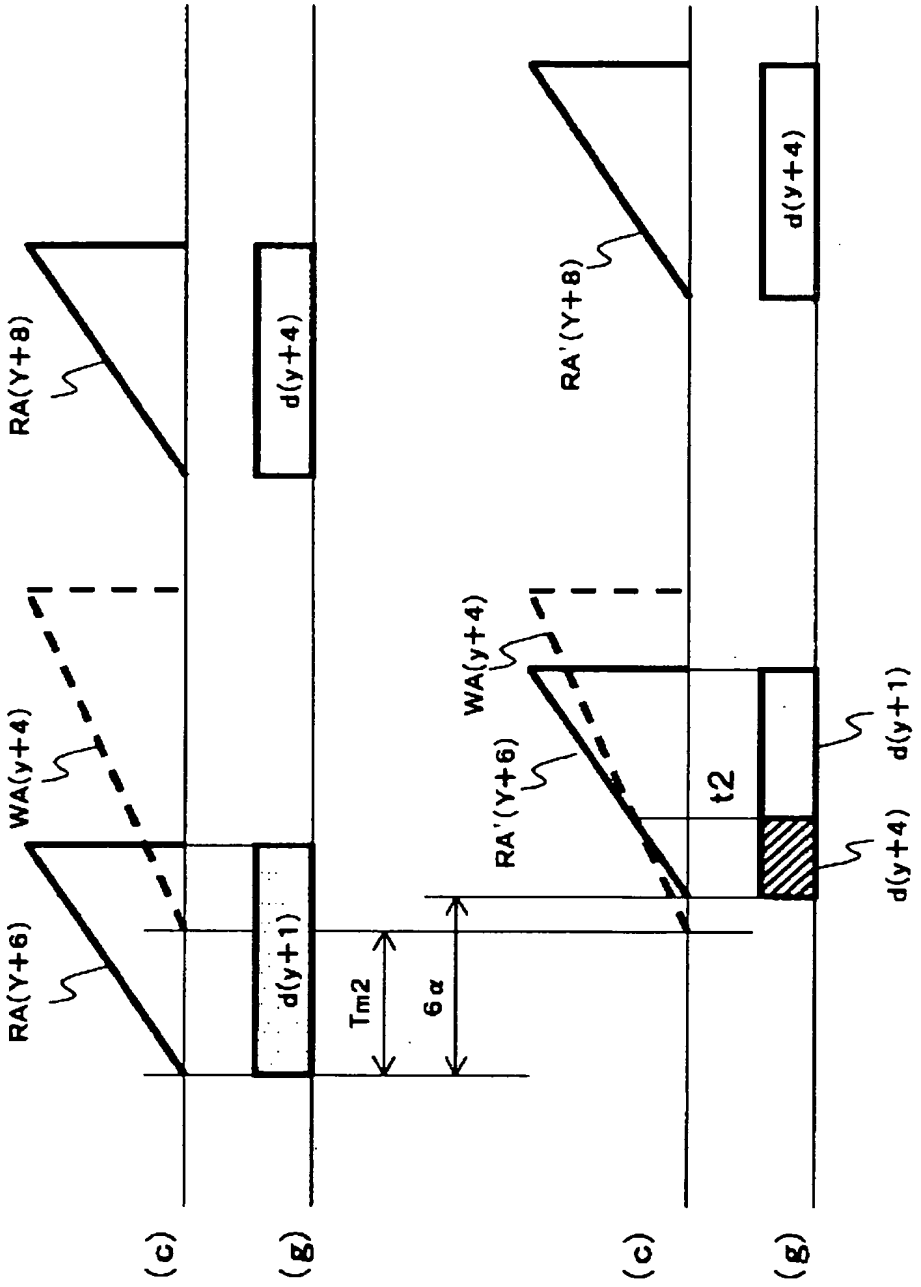

RA(Y+8)
d(y+4)
WA(y+4)
RA(Y+6)
d(y+1)
Tm2
6α
(c)
(g)
RA'(Y+8)
d(y+4)
WA(y+4)
RA'(Y+6)
t2
d(y+1)
d(y+4)
(c)
(g)

Fig. 9

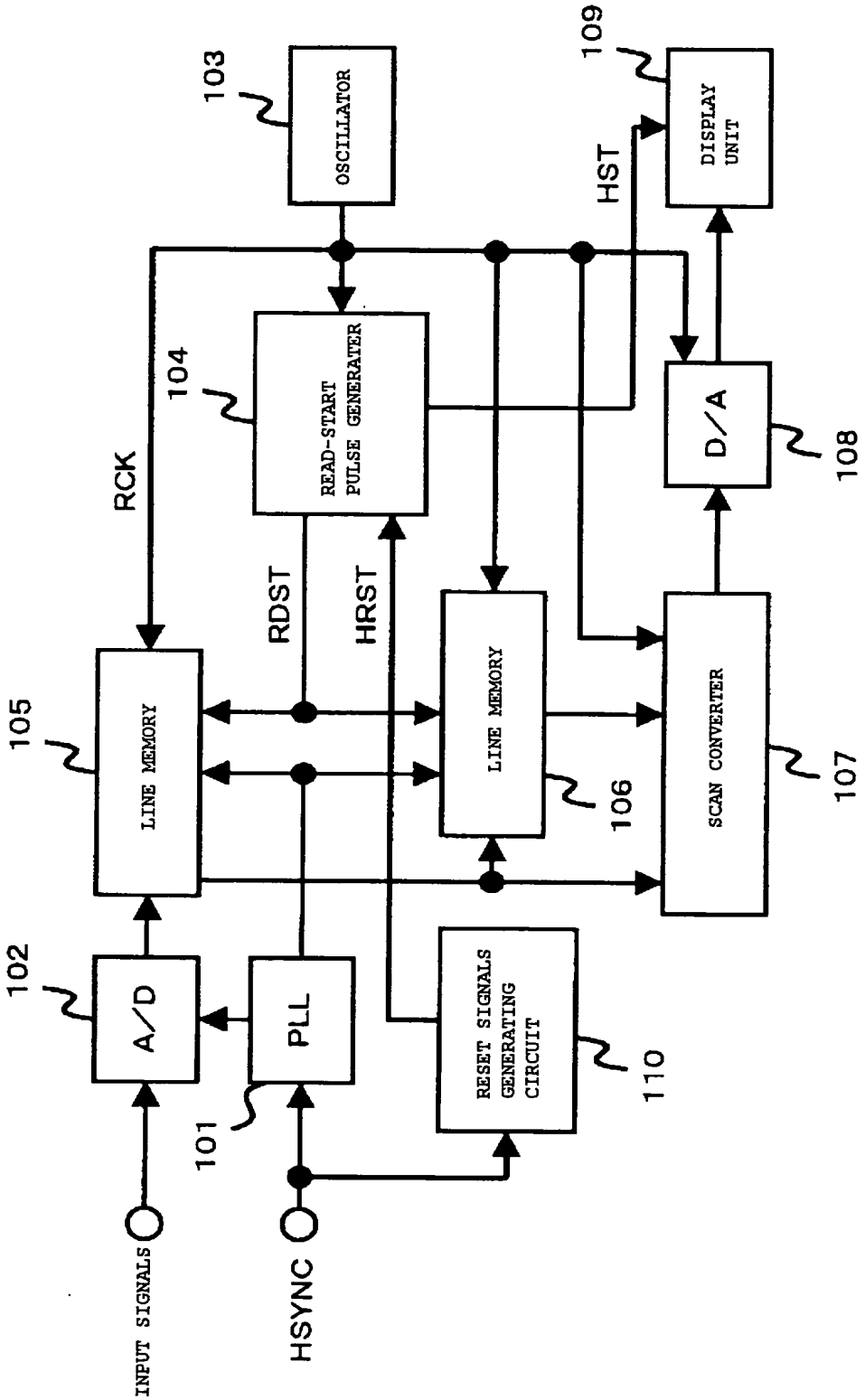

INPUT SIGNALS
HSYNC
A/D
PLL
LINE MEMORY
LINE MEMORY
SCAN CONVERTER
D/A
DISPLAY UNIT
OSCILLATOR
READ-START PULSE GENERATER
RESET SIGNALS GENERATING CIRCUIT
RCK
RDST
HRST
HST
101
102
103
104
105
106
107
108
109
110

Fig. 10

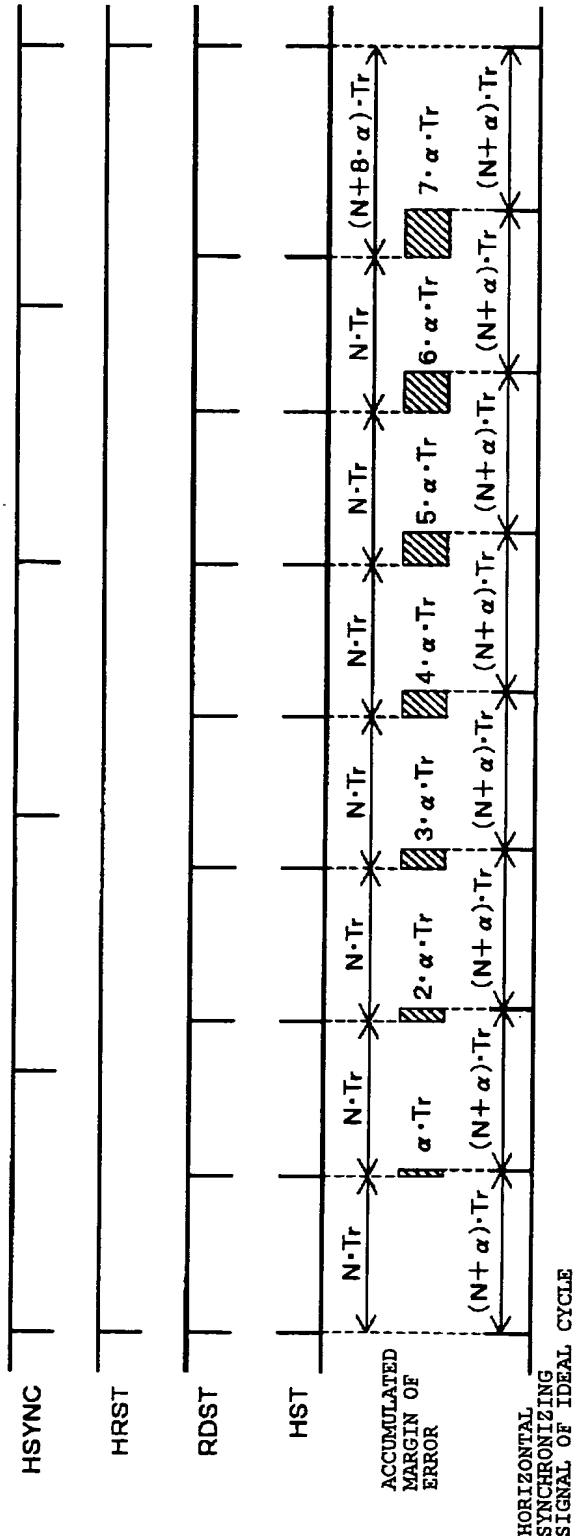
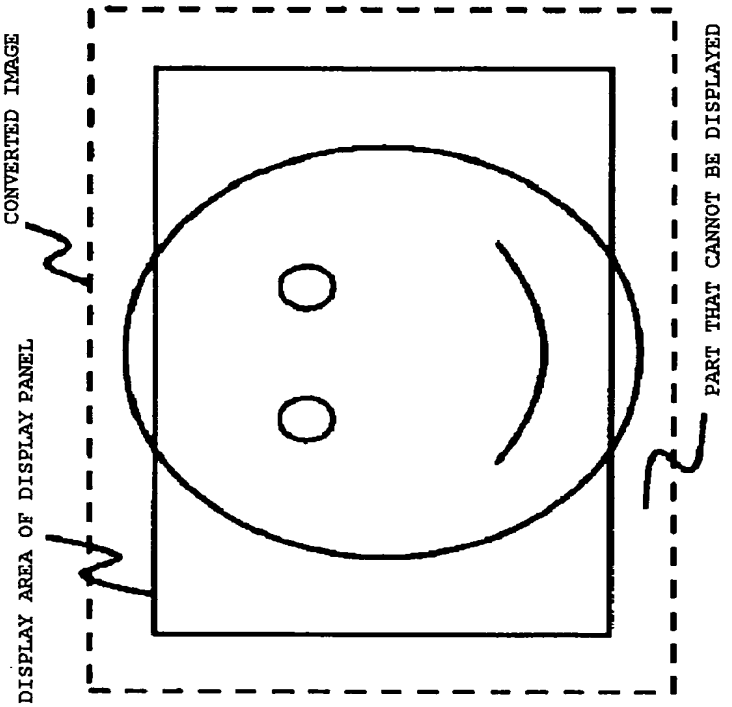
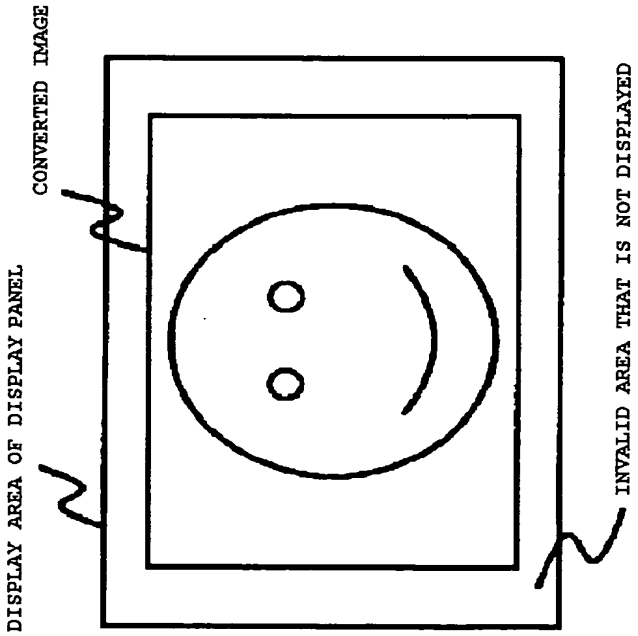

HSYNC
HRST
RDST
HST
ACCUMULATED MARGIN OF ERROR
HORIZONTAL SYNCHRONIZING SIGNAL OF IDEAL CYCLE
N·Tr
α·Tr
(N+α)·Tr
2·α·Tr
3·α·Tr
4·α·Tr
5·α·Tr
6·α·Tr
7·α·Tr
(N+8·α)·Tr

Fig. 11


CONVERTED IMAGE
DISPLAY AREA OF DISPLAY PANEL
PART THAT CANNOT BE DISPLAYED

(B)


CONVERTED IMAGE
DISPLAY AREA OF DISPLAY PANEL
INVALID AREA THAT IS NOT DISPLAYED

(A)

Fig. 12

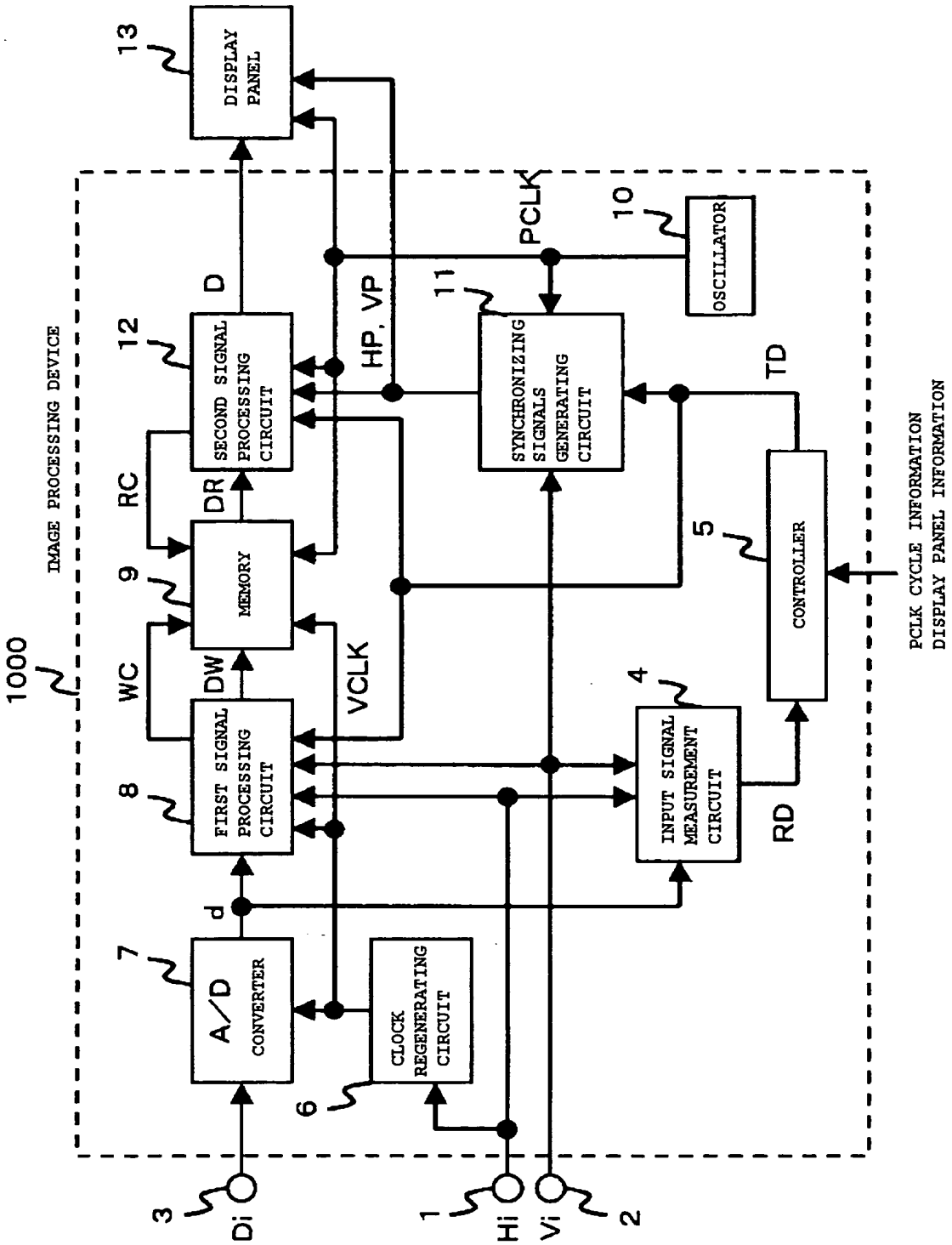

1000
IMAGE PROCESSING DEVICE
DISPLAY PANEL
13
SECOND SIGNAL PROCESSING CIRCUIT
12
D
HP, VP
PCLK
OSCILLATOR
10
SYNCHRONIZING SIGNALS GENERATING CIRCUIT
11
TD
RC
DR
MEMORY
9
CONTROLLER
5
WC
DW
VCLK
FIRST SIGNAL PROCESSING CIRCUIT
8
INPUT SIGNAL MEASUREMENT CIRCUIT
4
RD
d
A/D CONVERTER
7
CLOCK REGENERATING CIRCUIT
6
3
Di
1
Hi
Vi
2
PCLK CYCLE INFORMATION
DISPLAY PANEL INFORMATION

Fig. 13

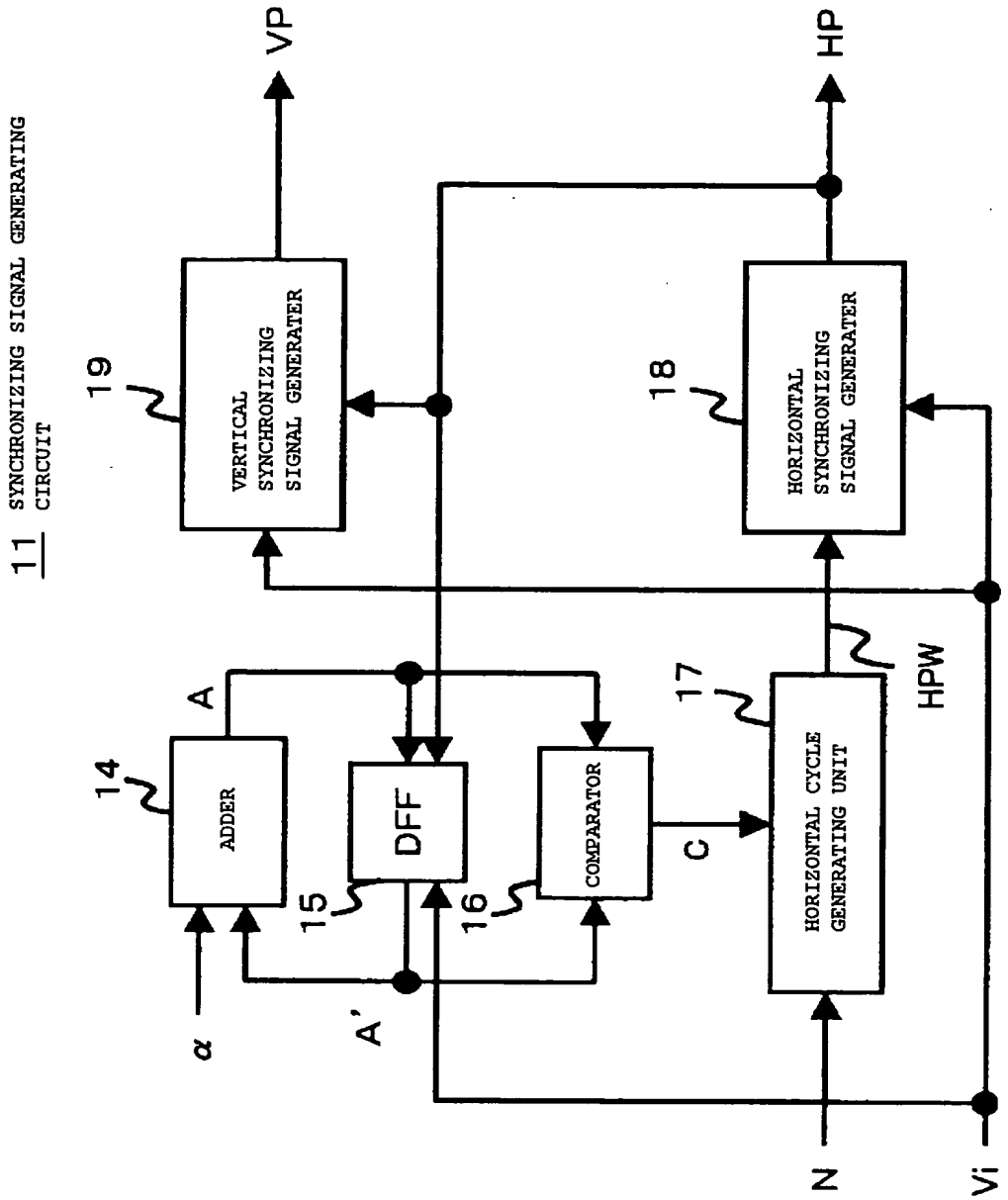

11 SYNCHRONIZING SIGNAL GENERATING CIRCUIT
VP
HP
19
VERTICAL SYNCHRONIZING SIGNAL GENERATER
18
HORIZONTAL SYNCHRONIZING SIGNAL GENERATER
A
14
ADDER
DFF
15
16
COMPARATOR
C
17
HORIZONTAL CYCLE GENERATING UNIT
HPW
α
A'
N
Vi

Fig. 14

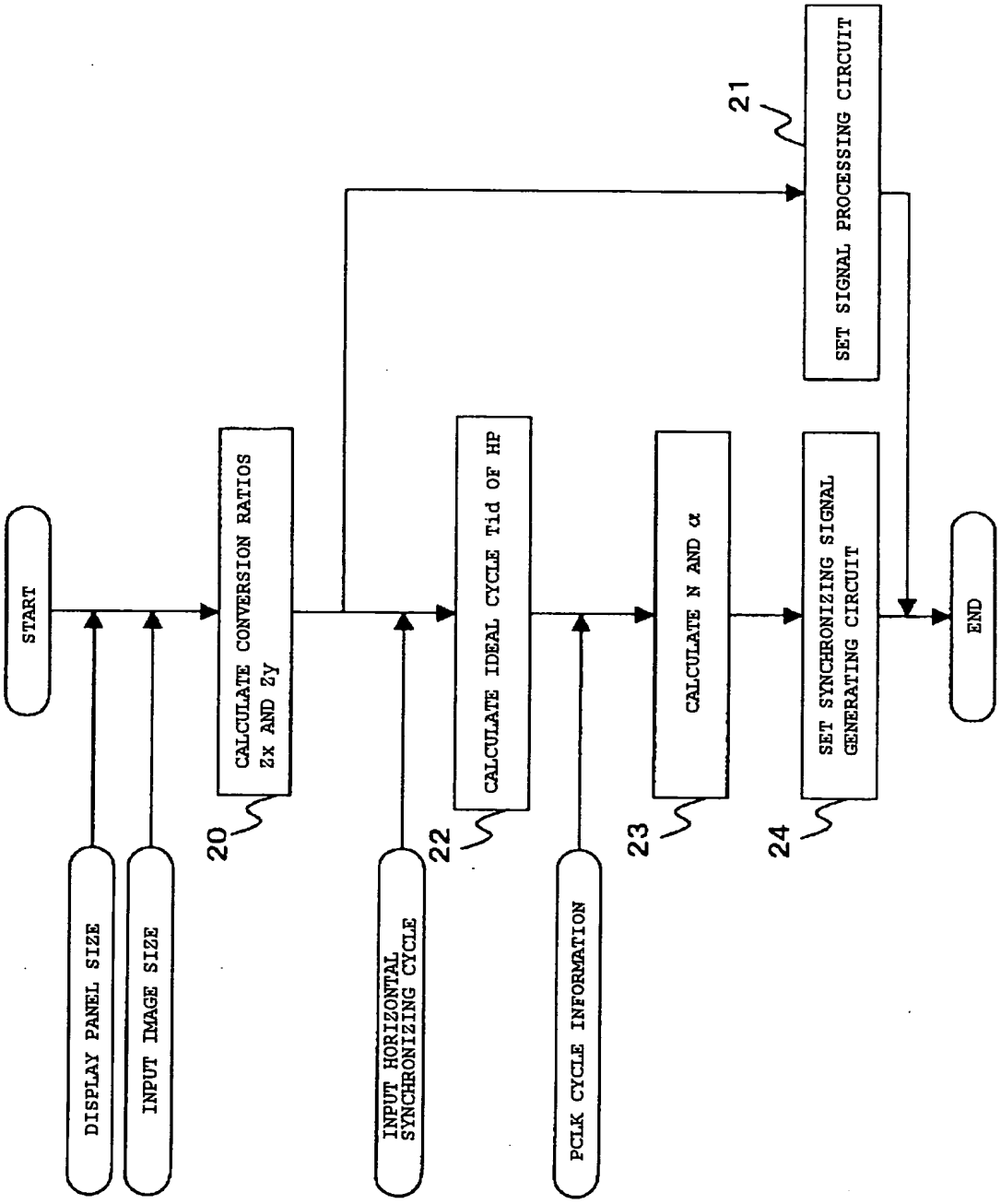

START
DISPLAY PANEL SIZE
INPUT IMAGE SIZE
CALCULATE CONVERSION RATIOS Zx AND Zy
20
INPUT HORIZONTAL SYNCHRONIZING CYCLE
CALCULATE IDEAL CYCLE Tid OF HP
22
PCLK CYCLE INFORMATION
CALCULATE N AND α
23
SET SYNCHRONIZING SIGNAL GENERATING CIRCUIT
24
21
SET SIGNAL PROCESSING CIRCUIT
END

Fig. 15

HORIZONTAL CONVERSION RATIO Zx	VERTICAL CONVERSION RATIO Zy	OPERATION MODE OF FIRST SIGNAL PROCESSING CIRCUIT	OPERATION MODE OF SECOND SIGNAL PROCESSING CIRCUIT
$Zx \geqq 1$ (ENLARGE)	$Zy \geqq 1$ (ENLARGE)	THROUGH	HORIZONTAL ENLARGEMENT, VERTICAL ENLARGEMENT
$Zx \geqq 1$ (ENLARGE)	$Zy < 1$ (REDUCE)	THROUGH	HORIZONTAL ENLARGEMENT, VERTICAL REDUCTION
$Zx < 1$ (REDUCE)	$Zy \geqq 1$ (ENLARGE)	HORIZONTAL REDUCTION	VERTICAL ENLARGEMENT, (HORIZONTAL THROUGH)
$Zx < 1$ (REDUCE)	$Zy < 1$ (REDUCE)	HORIZONTAL REDUCTION	VERTICAL REDUCTION, (HORIZONTAL THROUGH)

Fig. 16

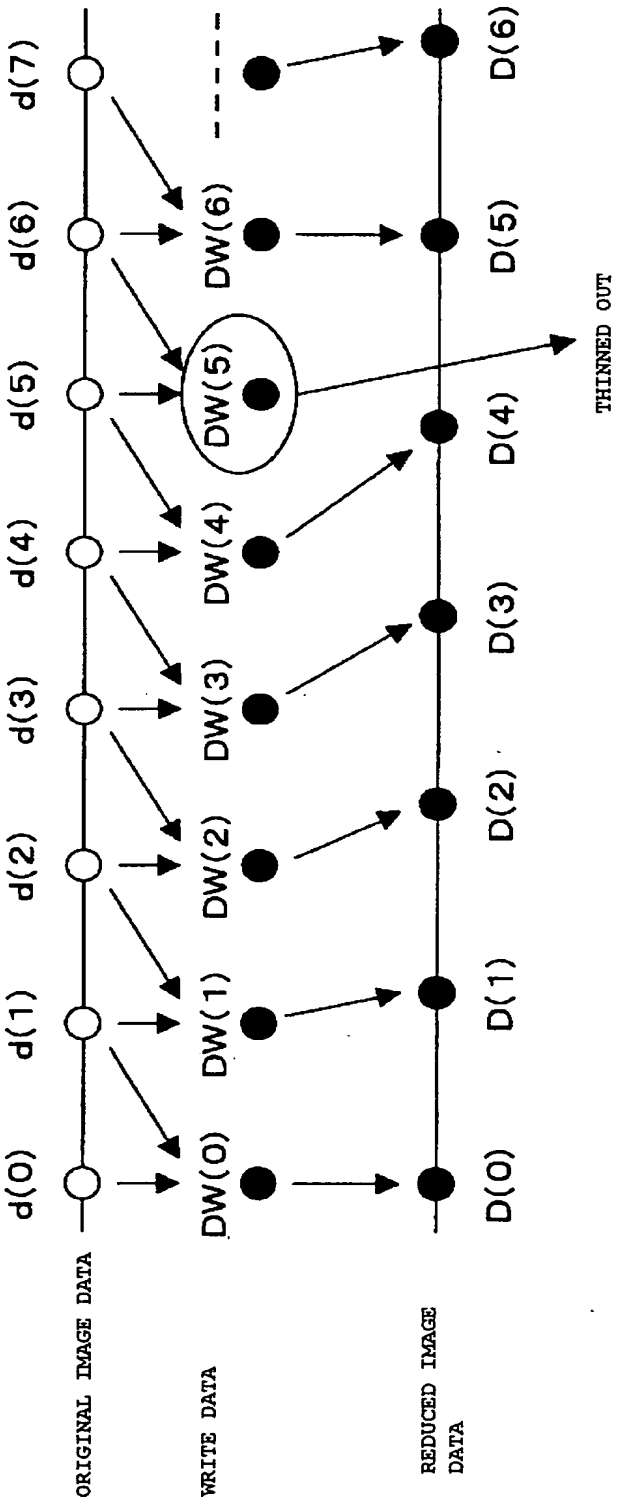

d(0)
d(1)
d(2)
d(3)
d(4)
d(5)
d(6)
d(7)
ORIGINAL IMAGE DATA
DW(0)
DW(1)
DW(2)
DW(3)
DW(4)
DW(5)
DW(6)
WRITE DATA
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
REDUCED IMAGE DATA
THINNED OUT

Fig. 17

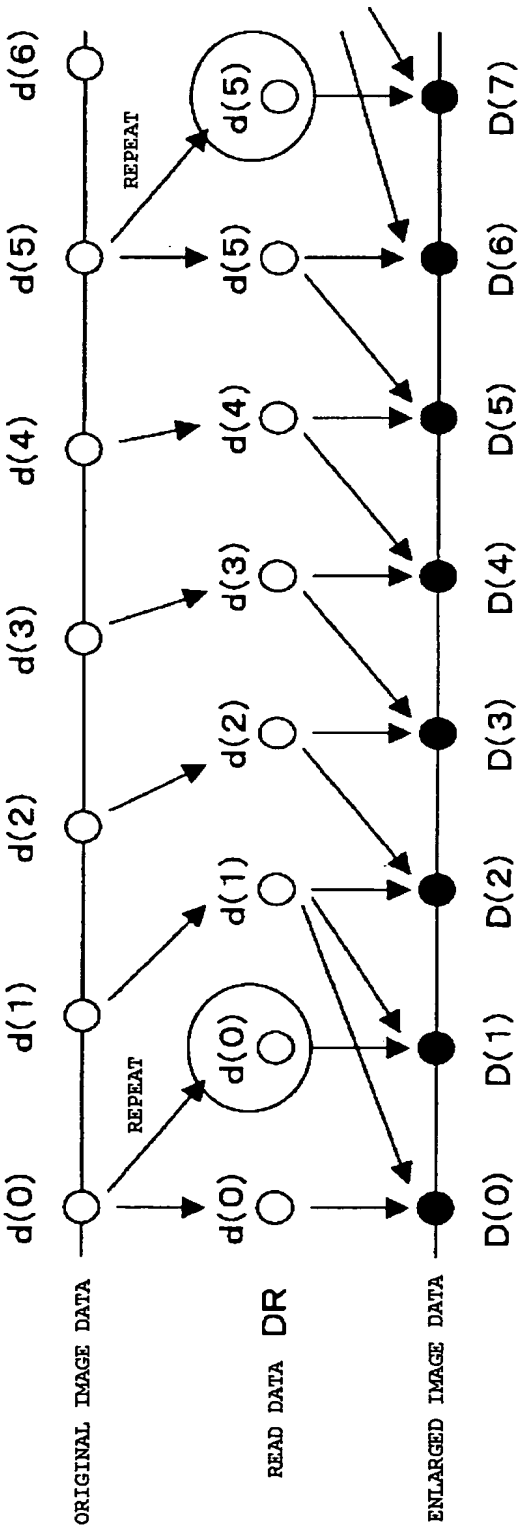

ORIGINAL IMAGE DATA
d(0)
d(1)
d(2)
d(3)
d(4)
d(5)
d(6)
REPEAT
REPEAT
READ DATA DR
d(0)
d(0)
d(1)
d(2)
d(3)
d(4)
d(5)
d(5)
ENLARGED IMAGE DATA
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)

Fig. 18

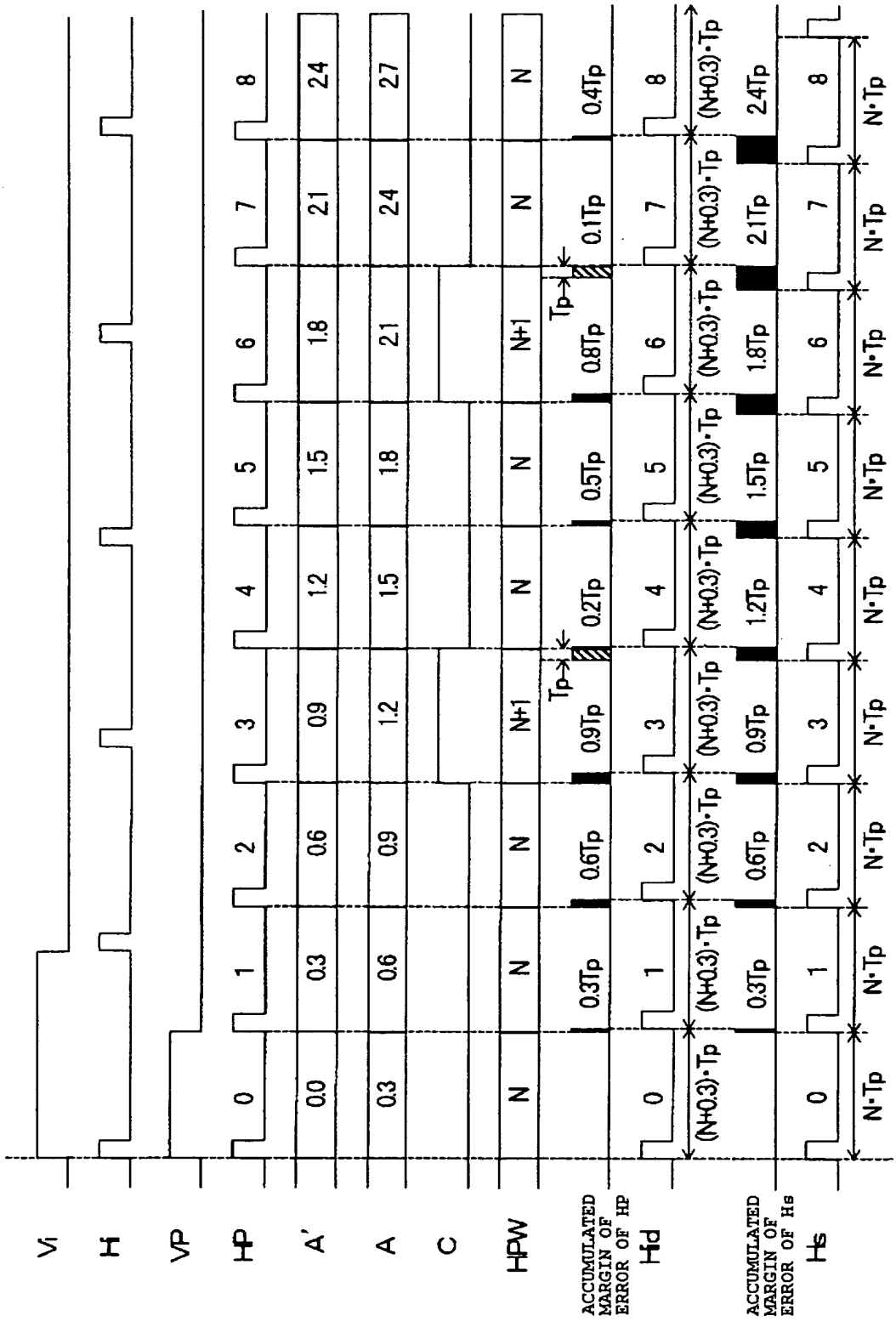

Vi
H
VP
HP
A'
A
C
HPW
ACCUMULATED MARGIN OF ERROR OF HP
Hd
ACCUMULATED MARGIN OF ERROR OF Hd
Hs
Tp
0.3Tp
0.6Tp
0.9Tp
0.2Tp
0.5Tp
0.8Tp
0.1Tp
0.4Tp
(N+0.3)·Tp
N·Tp
0.0
0.3
0.6
0.9
1.2
1.5
1.8
2.1
2.4
2.7
N
N+1

Fig. 19

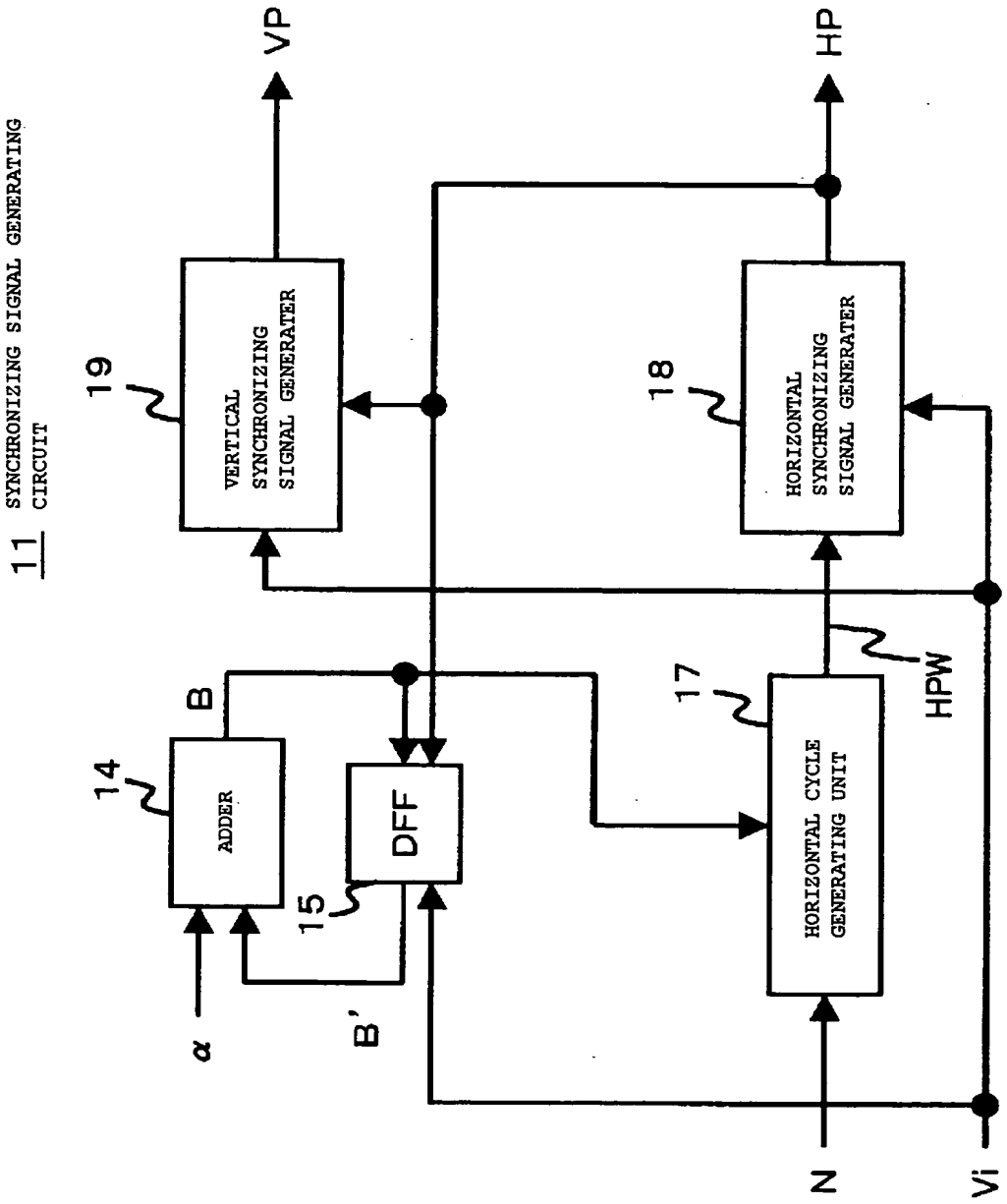

11 SYNCHRONIZING SIGNAL GENERATING CIRCUIT
VP
HP
19
VERTICAL SYNCHRONIZING SIGNAL GENERATER
18
HORIZONTAL SYNCHRONIZING SIGNAL GENERATER
B
14
ADDER
DFF
15
17
HORIZONTAL CYCLE GENERATING UNIT
HPW
α
B'
N
Vi

Fig. 20

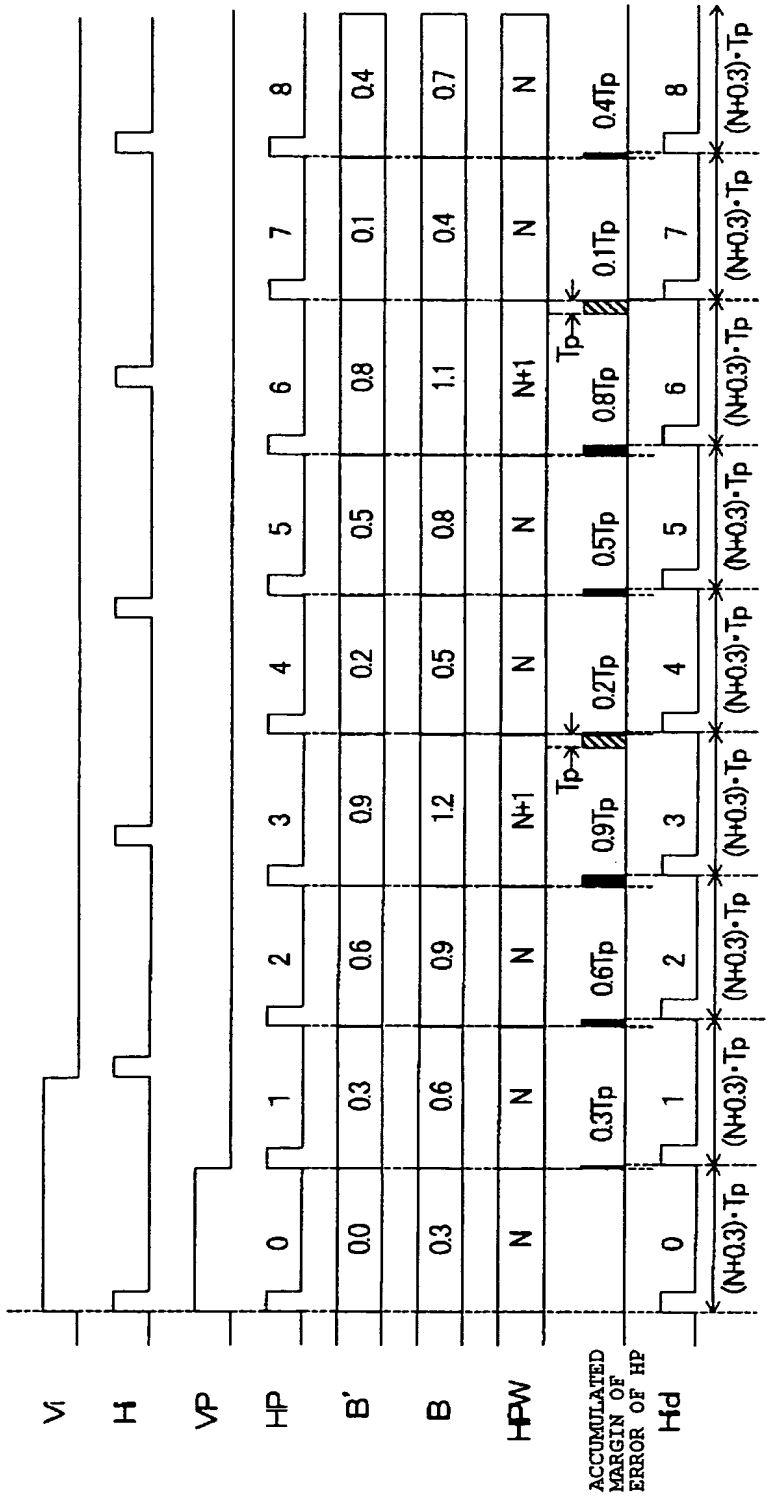

Vi
H
VP
HP
B'
B
HPW
ACCUMULATED MARGIN OF ERROR OF HP
Hd
0
1
2
3
4
5
6
7
8
0.0
0.3
0.6
0.9
1.2
0.5
0.8
1.1
0.4
0.7
N
N+1
0.3Tp
0.6Tp
0.9Tp
0.2Tp
0.5Tp
0.8Tp
0.1Tp
0.4Tp
Tp
(N+0.3)·Tp

Fig. 21

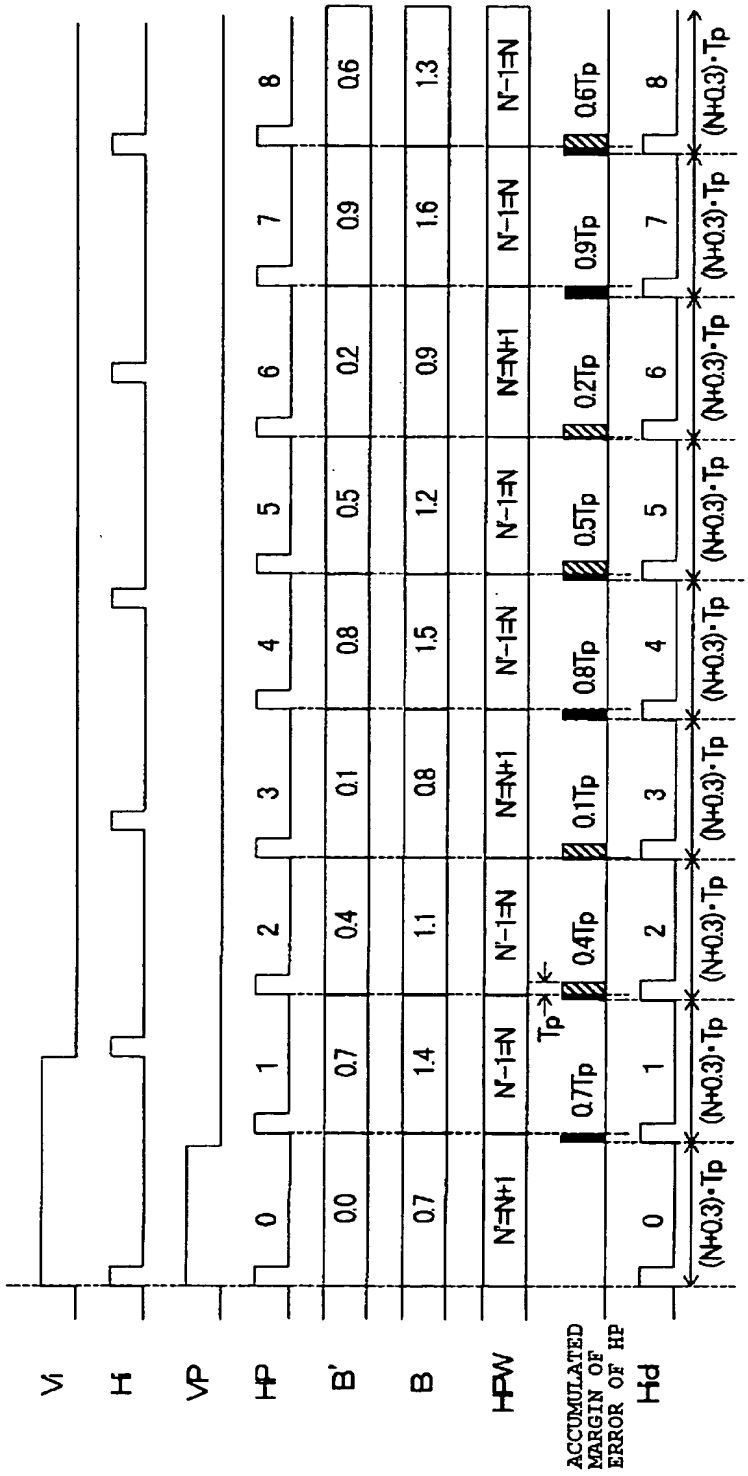

Vi
Hi
VP
HP
B'
B
HPW
ACCUMULATED MARGIN OF ERROR OF HP
Hd
N'=N+1
N'-1=N
0.7Tp
0.4Tp
0.1Tp
0.8Tp
0.5Tp
0.2Tp
0.9Tp
0.6Tp
Tp
(N+0.3)·Tp
0
1
2
3
4
5
6
7
8
0.0
0.7
1.4
0.4
1.1
0.1
0.8
1.5
0.8
1.2
0.5
0.9
0.2
1.6
0.9
1.3

Fig. 22

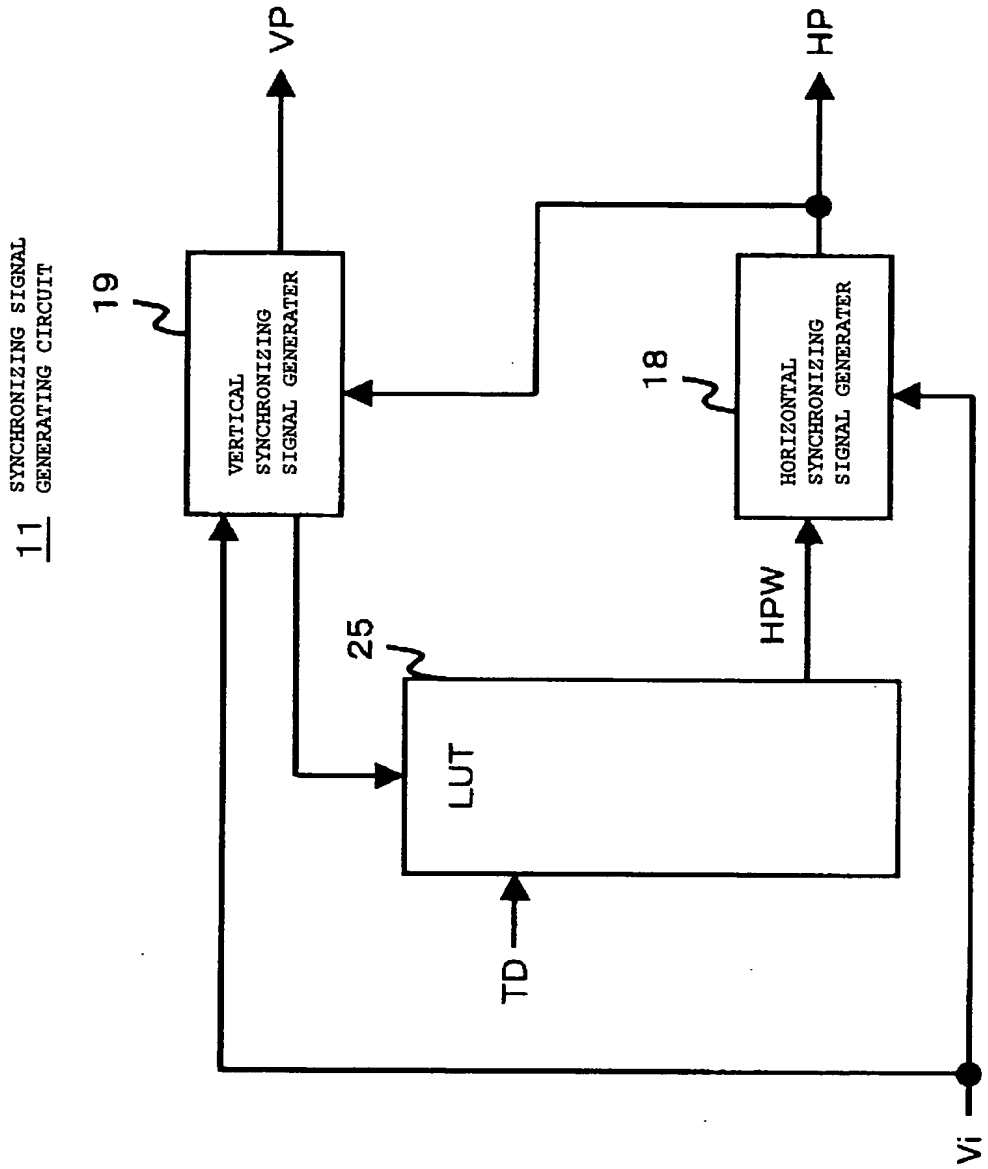

11 SYNCHRONIZING SIGNAL GENERATING CIRCUIT
19
VERTICAL SYNCHRONIZING SIGNAL GENERATER
18
HORIZONTAL SYNCHRONIZING SIGNAL GENERATER
25
LUT
VP
HP
HPW
TD
Vi

Fig. 23

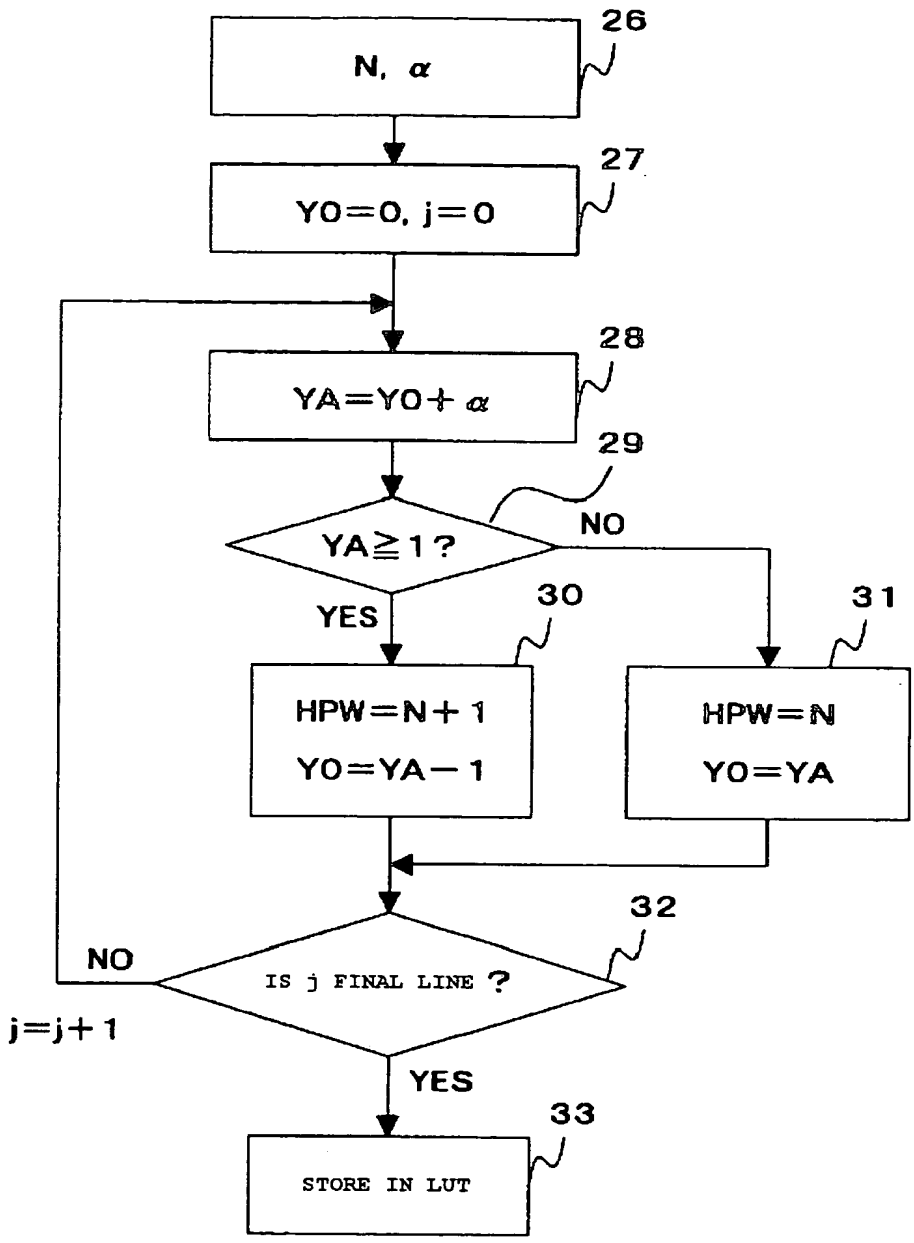

N, α
26
Y0=0, j=0
27
YA=Y0+α
28
YA≧1?
29
NO
YES
30
31
HPW=N+1
Y0=YA−1
HPW=N
Y0=YA
IS j FINAL LINE ?
32
NO
j=j+1
YES
STORE IN LUT
33

Fig. 24

ADDRESS	DATA HPW
0	N
1	N
2	N
3	N+1
4	N
5	N
6	N+1
7	N
8	N
:	:
:	:
:	:

Fig. 25

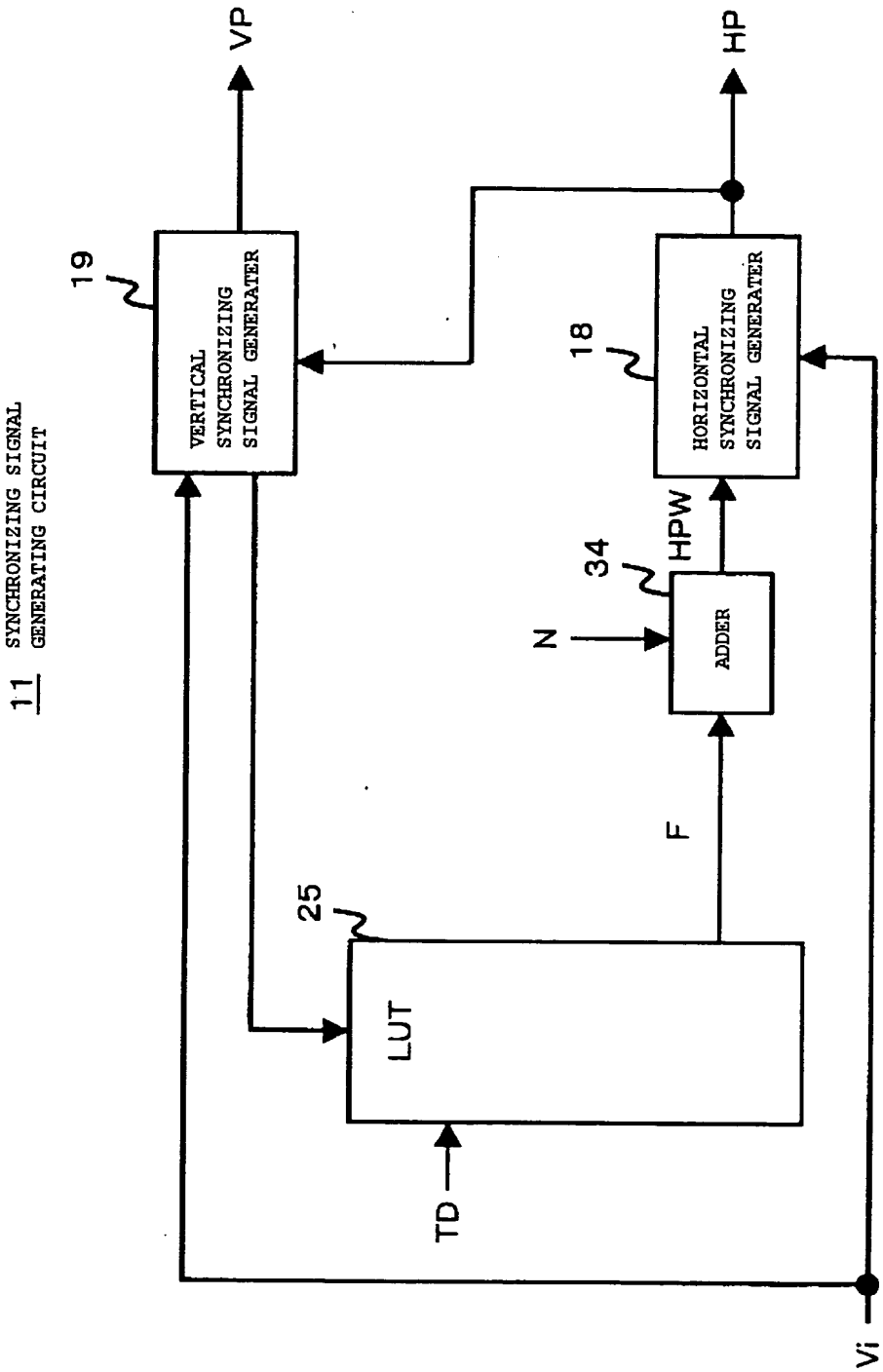

11 SYNCHRONIZING SIGNAL GENERATING CIRCUIT
VP
HP
19
VERTICAL SYNCHRONIZING SIGNAL GENERATER
18
HORIZONTAL SYNCHRONIZING SIGNAL GENERATER
HPW
34
N
ADDER
F
25
LUT
TD
Vi

Fig. 26

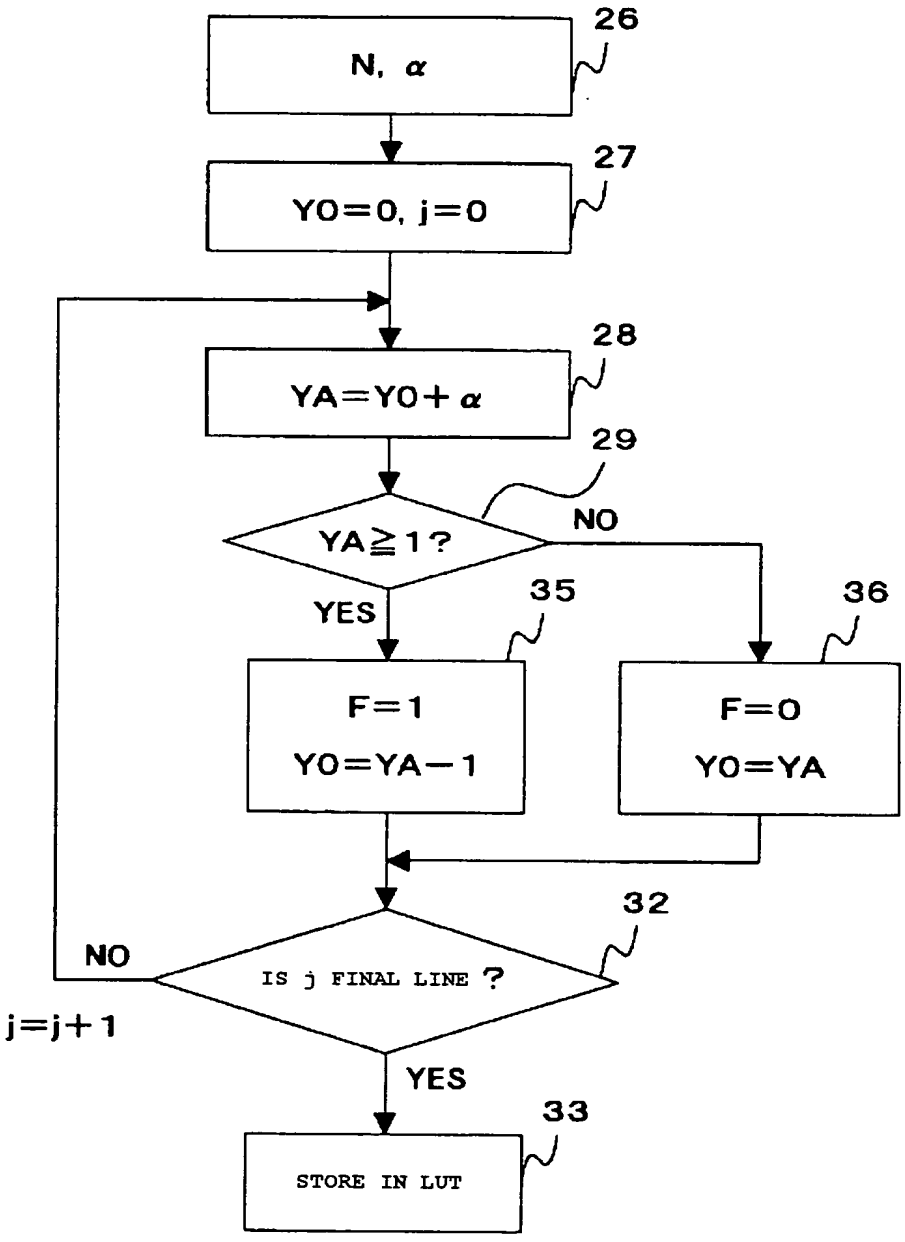

N, α
26
Y0=0, j=0
27
YA=Y0+α
28
YA≧1?
29
NO
YES
35
36
F=1
Y0=YA−1
F=0
Y0=YA
32
NO
IS j FINAL LINE ?
j=j+1
YES
33
STORE IN LUT

Fig. 27

ADDRESS	DATA F
0	0
1	0
2	0
3	1
4	0
5	0
6	1
7	0
8	0
:	:
:	:
:	:

Fig. 28

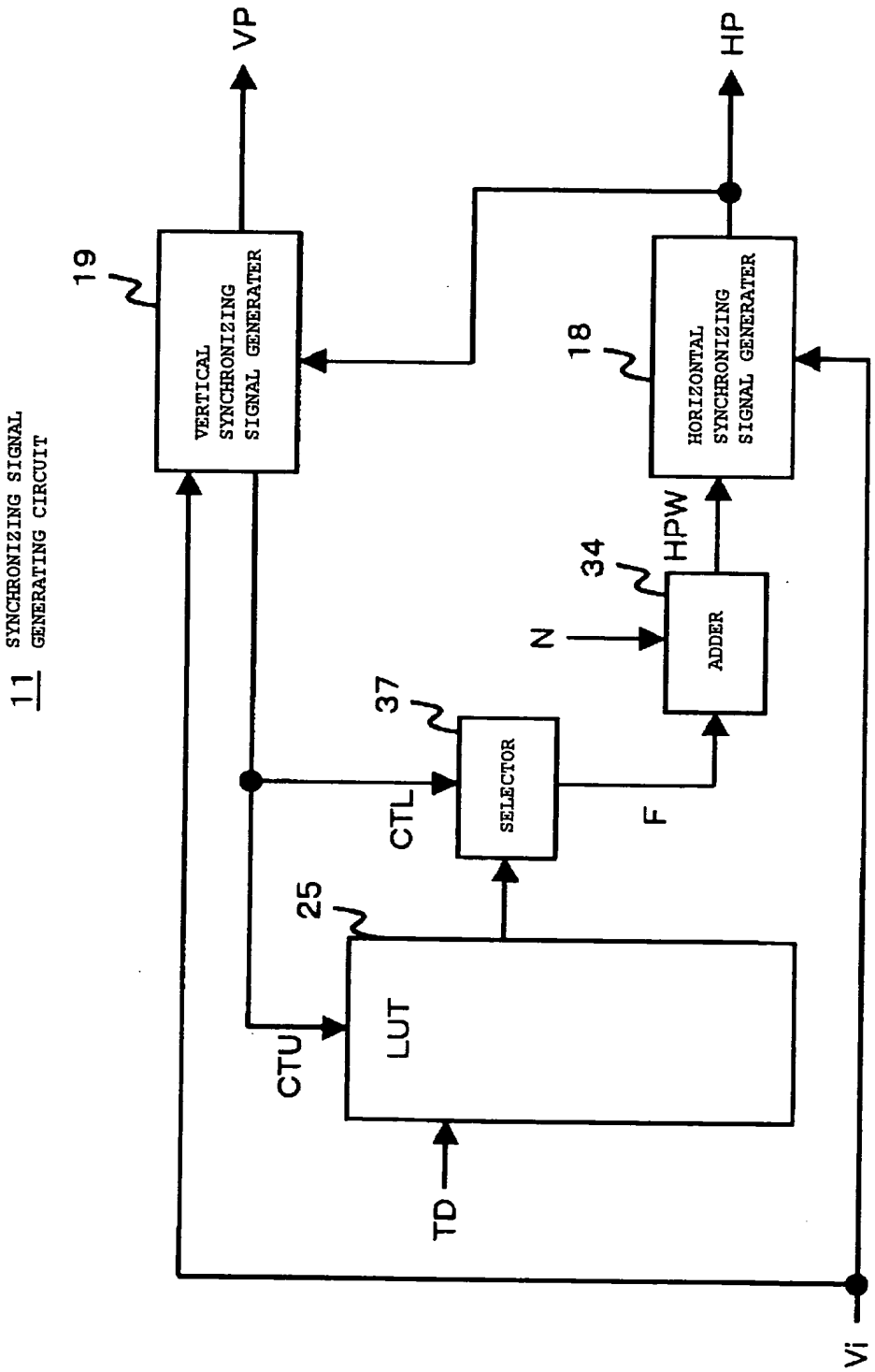
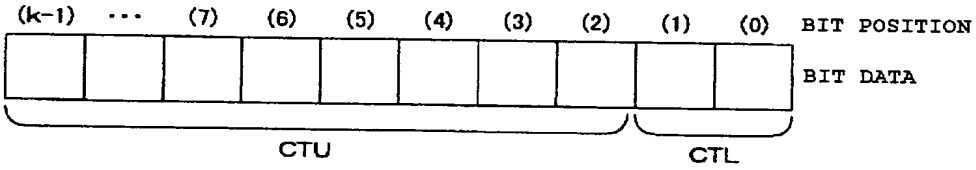

11 SYNCHRONIZING SIGNAL GENERATING CIRCUIT
VP
HP
19
VERTICAL SYNCHRONIZING SIGNAL GENERATER
18
HORIZONTAL SYNCHRONIZING SIGNAL GENERATER
34
HPW
N
ADDER
37
CTL
SELECTOR
F
25
CTU
LUT
TD
Vi

Fig. 29

ADDRESS	DATA b3	DATA b2	DATA b1	DATA b0
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	1	0
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:

(a)



(b)

LINE COUNT RESULTS	CTU	CTL
0	0	0
1	0	1
2	0	2
3	0	3
4	1	0
5	1	1
6	1	2
7	1	3
8	2	0
9	2	1
10	2	2
11	2	3
:	:	:

(c)

Fig. 30

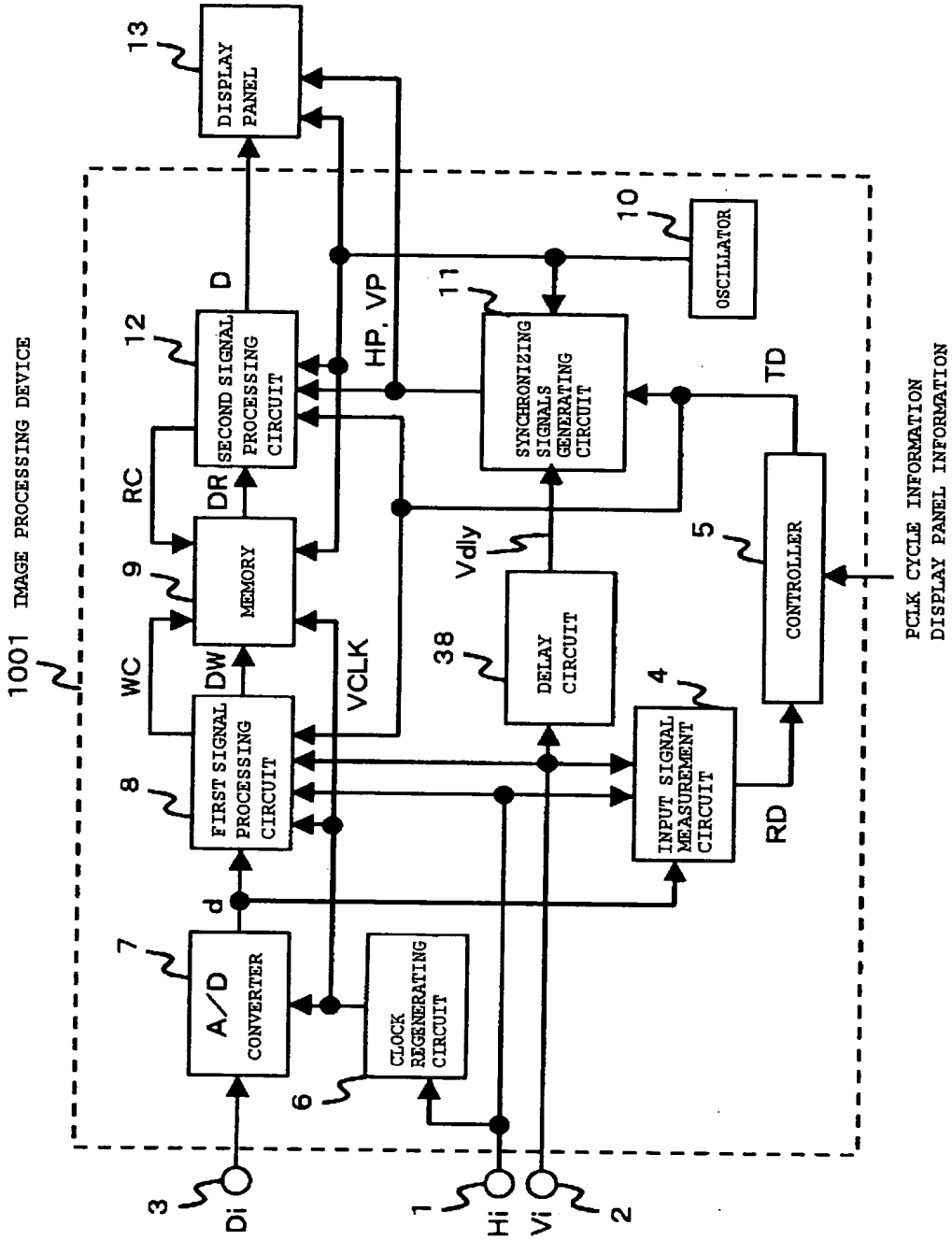

1001 IMAGE PROCESSING DEVICE
13 DISPLAY PANEL
12 SECOND SIGNAL PROCESSING CIRCUIT
D
HP, VP
11 SYNCHRONIZING SIGNALS GENERATING CIRCUIT
10 OSCILLATOR
TD
RC
DR
9 MEMORY
Vdly
38 DELAY CIRCUIT
5 CONTROLLER
WC
DW
VCLK
8 FIRST SIGNAL PROCESSING CIRCUIT
4 INPUT SIGNAL MEASUREMENT CIRCUIT
RD
d
7 A/D CONVERTER
6 CLOCK REGENERATING CIRCUIT
3 Di
1 Hi
Vi 2
PCLK CYCLE INFORMATION
DISPLAY PANEL INFORMATION

Fig. 31

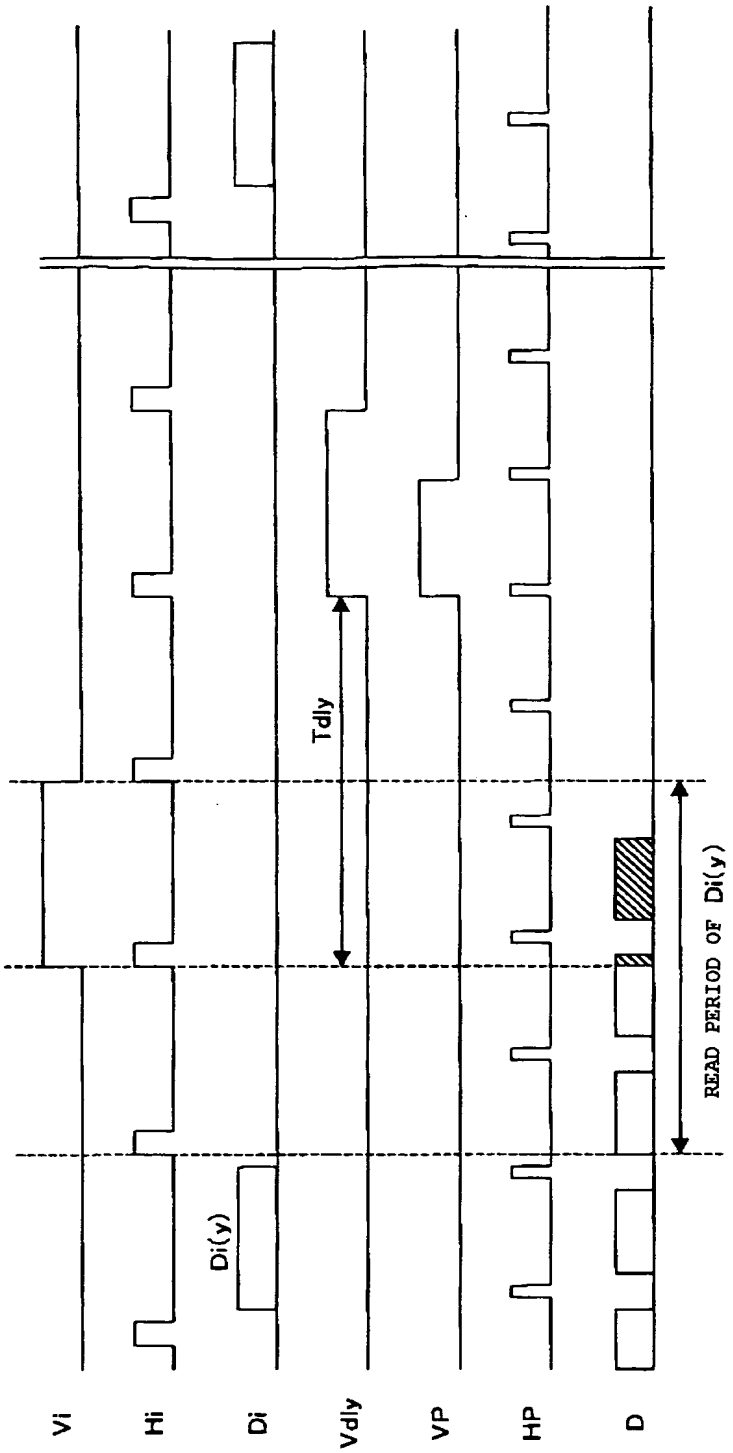


Fig. 32

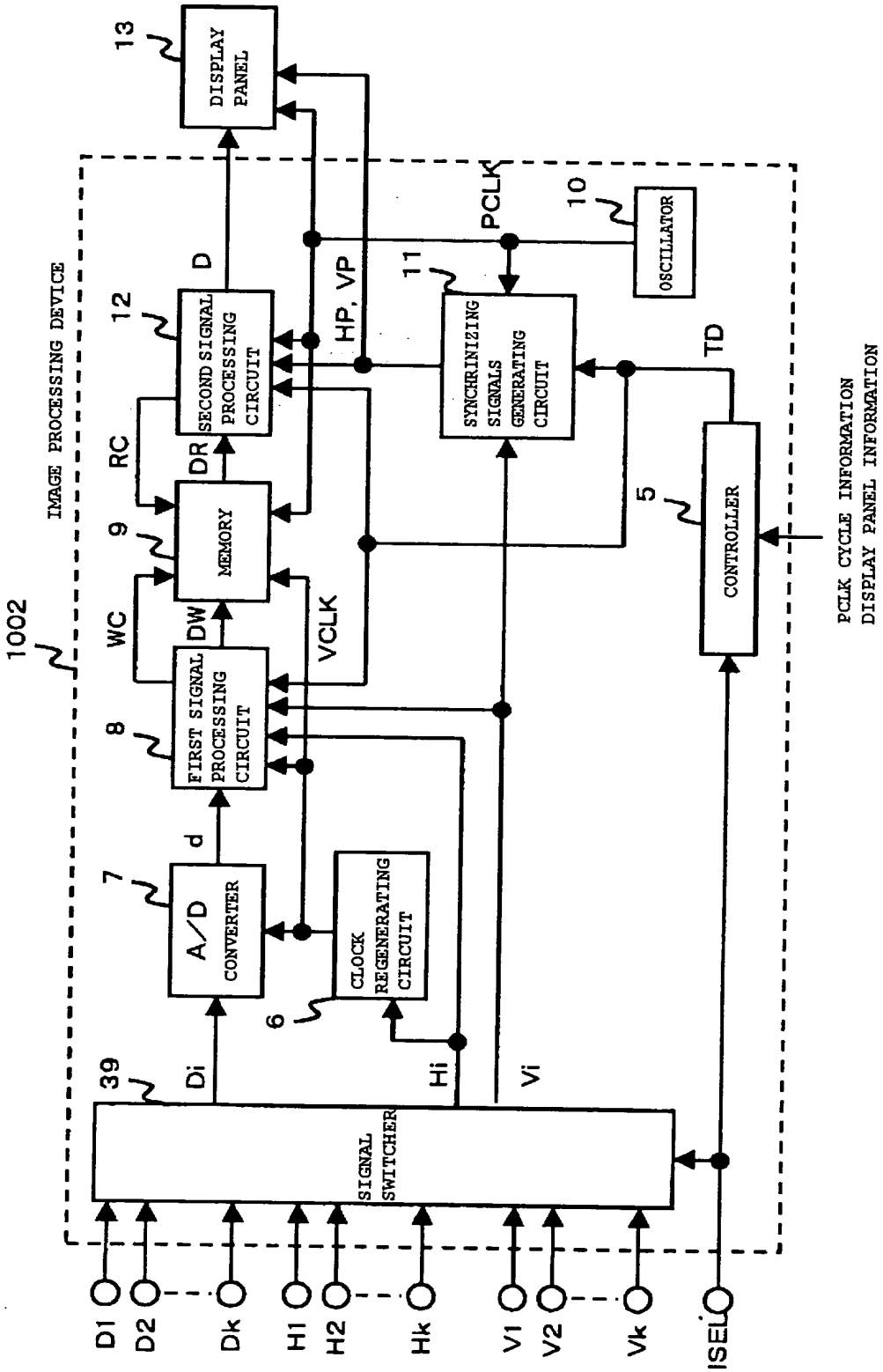


IMAGE PROCESSING DEVICE
1002
13
DISPLAY PANEL
12
SECOND SIGNAL PROCESSING CIRCUIT
D
HP, VP
PCLK
10
OSCILLATOR
11
SYNCHRINIZING SIGNALS GENERATING CIRCUIT
TD
RC
DR
9
MEMORY
5
CONTROLLER
WC
DW
VCLK
8
FIRST SIGNAL PROCESSING CIRCUIT
d
7
A/D CONVERTER
6
CLOCK REGENERATING CIRCUIT
39
Di
Hi
Vi
SIGNAL SWITCHER
D1
D2
Dk
H1
H2
Hk
V1
V2
Vk
ISEL
PCLK CYCLE INFORMATION
DISPLAY PANEL INFORMATION